designer's manual

SYSTEM 74

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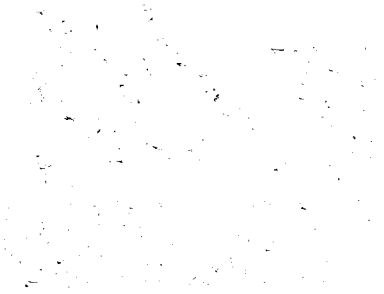


Introduction

SYSTEM 74 INTRODUCTION

System 74 is a new look at logic design.

Texas Instruments have the justifiable reputation for anticipating the needs of designers with the continued introduction of technically innovative devices. To complement this technical capability we now introduce System 74. *The* most comprehensive service to designers of logic equipment. It is your guarantee of quality, reliability, economy and service, and is available only from Texas Instruments Ltd. and the approved System 74 Distributors.

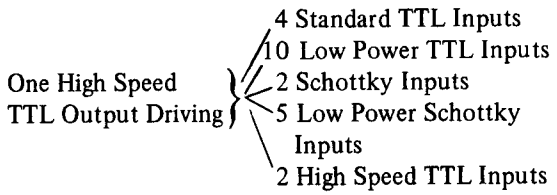
System 74 starts with a range of over 300 TTL and TTL compatible devices from these 6 major families:

SN74N	Standard TTL
SN74LN	Low Power TTL
SN74LSN	Low Power Schottky TTL
SN74HN	High Speed TTL
SN74SN	High Speed Schottky TTL
SN75N	TTL Compatible Interface.

But System 74 is more than just this.

Logic design is complex. To optimise your systems for speed, power, reliability, and economy, you will want to mix all the families contained in System 74.

Take an example



This immediately poses some questions:–

1. Will it work?
2. How can I compute the loading?
3. How reliable will it be?
4. Can I modify it?
5. Can I buy all the devices from one source and can I be sure that they will be compatible?

This Manual shows a way of answering these questions in minutes. It contains full information on devices and pin-outs, and extensive sections on the application of TTL and interface devices. Also included are sections on quality and reliability together with a unique method of computing inter-family loading.

In the unlikely event that you find a question that cannot be answered by this manual the System 74 Technical Enquiry Service is now available at Texas Instruments–Dial Bedford 67466, ask for System 74 and you will be connected to the World's largest semiconductor manufacturers.

System 74 is also a new pricing concept. For the first time the Design Engineer is given mixed pricing on list price quantities *across all the families.*

Now you can buy all your devices on the same order and qualify for the price of the total quantity mix.

This not only saves money but simplifies purchases on Design Quantities. We call it "One Stop Shopping" and think you will find this a great advantage.

The field of logic design will continue to grow with the introduction of new technologies and more complex devices. System 74 will keep you up to date with all these developments as they happen. Ask us to add your name to the System 74 mailing list by completing the card at the back of this book.

Technical Aspects

TECHNICAL ASPECTS OF SYSTEM 74

As suggested in the introduction to this manual, System 74 allows the designer to readily select from around 300 TTL compatible functions. In order to make this an attractive and practical philosophy, the basic characteristics and parameters of the individual families comprehended in System 74 are presented in this manual to allow the reader to make a comparative evaluation of the five TTL ranges available. The information presented does not replace the comprehensive data sheets available but is intended to outline the basic compatibility of all 74 series TTL products and their relationship to the 75 series of interface devices.

The basic family in System 74 is the SN 74N series transistor – transistor logic, and a thorough discussion of the history and evolution of this popular form of digital integrated circuit logic is given in Application Report B124. The complete range of product included in System 74 is contained in the Selection Guide section of this manual.

All System 74 products are offered in the commercial $0^{o}C$ to $70^{o}C$ operating temperature range and are packaged in "plastic" dual-in-line N Pack. The product ranges included are as follows:-

SN74N	Standard TTL
SN74LN	Low power TTL
SN74LSN	Low power Schottky TTL
SN74HN	High speed TTL
SN74SN	Schottky TTL
SN75N	Interface devices

The SN74 series ranges have basically similar circuit design, logic capability and operate on similar voltage levels. The differences are those of speed and power dissipation. For example, SN74LN has very low dissipation and hence has a low speed of operation, and SN74SN is fast and consumes a greater power. This can be summarised as in Table 1 using typical gate characteristics for power dissipation and propagation delays:-

PARAMETER	74L	74L*	74LS	74	74H	74S	UNIT
Typical Propagation Delay	33	20	10	10	6	3	ns
Typical Power Dissipation	1	5	2	10	22	20	mW
Speed/Power Product	33	100	20	100	132	60	pj
Flip-Flop Clock Input Frequency Range	DC to 3 MHz	DC to 20 MHz	DC to 45 MHz	DC to 35 MHz	DC to 50 MHz	DC to 125 MHz	

NOTE: SN74L*N devices are those low power products derived from SN74 series which are half-power versions of the standard products. These are identified in the selection guide by use of asterisks.

The speed/power product in picojoules is a commonly accepted figure of merit for integrated circuit families obtained by multiplying typical propagation delay in nanoseconds by typical power dissipation in milliwatts. As would be expected the most recently designed families are demonstrably improving this measure, (with 74LS at 20 picojoules offering the best speed/power product). It should be remembered that speed/power product is derived from typical gate parameters and that complex functions can improve this considerably. Thus, a speed/power product for a System 74 system using principally complex functions will be better than an equivalent system built using gates.

SN75 series includes functions such as line drivers and line receivers, memory drivers, sense amplifiers, and peripheral drivers to provide TTL compatible interfaces with transmission lines, core and MOS memories, and simple interfaces to relays, lamps and other electromechanical devices. All SN75 series products specified in the selection guide have SN74 series compatible inputs or outputs, as relevant, and with few exceptions have parameters similar to standard SN74 TTL.

Before deriving and considering the D.C. parameters of System 74 TTL families the significance and notation of these parameters will be discussed.

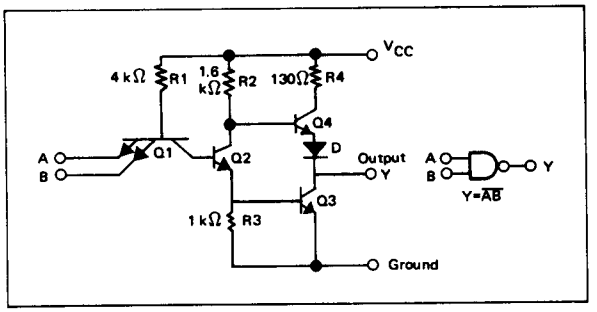


Fig. 2. Schematic diagram and logic symbol for SN74 NAND gate.

The output shown for this gate is similar to all active pullup output devices throughout System 74 and is subject to two voltage parameters.

V_{OL} is maximum low state output voltage when driving full load (i.e. maximum fan-out)

V_{OH} is minimum high state output voltage when driving full load (i.e. maximum fan-out)

These parameters, thus, fully determine the worst-case voltage swing of the output.

The inputs are similarly subjected to voltage parameters.

V_{IL} is maximum input voltage guaranteed to appear as a low state input voltage.

V_{IH} is minimum input voltage guaranteed to appear as a high state input voltage.

These parameters fully determine the worst case voltage operating thresholds of an input. All voltages are positive w.r.t. the ground or zero voltage terminal.

The voltages are accompanied by current parameters, which obey the following convention. Currents flowing into inputs or outputs are positive and those flowing out of inputs or outputs are negative.

I_{OL} is maximum positive current into a low state output at not more the V_{OL}

I_{OH} is maximum negative current out of a high state output at not lower than V_{OH}

These parameters indicate the capability of an output to drive inputs of other functions.

I_{IL} is maximum negative current out of an input held at V_{OL}

I_{IH} is maximum positive current into an input held at V_{OH}

These parameters indicate the input requirements with worst case driving voltages.

Other parameters and operating conditions are specified in the data sheet and once again Application Report B124 provides excellent background.

The basic parameters outlined above will be used to compare the families in System 74 to estimate worst case noise immunities and drive capability and demonstrate the basic compatibility that exists across all System 74 TTL families.

SYSTEM 74 D.C. PARAMETERS

	SN74L	SN74L*	SN74LS	SN74	SN74H	SN74S	UNITS
V_{OL}	0.3	0.4	0.5	0.4	0.4	0.5	V
V_{OH}	2.4	2.4	2.7	2.4	2.4	2.7	V
I_{OL}	2.0	8.0	8.0	16.00	20.00	20.00	mA
I_{OH}	-200	-400	-400	-400	-500	-1000	μA
V_{IL}	0.7	0.8	0.8	0.8	0.8	0.8	V
V_{IH}	2.0	2.0	2.0	2.0	2.0	2.0	V
I_{IL}	-0.18	-0.8	-0.36	-1.6	-2.0	-2.0	mA
I_{IH}	10.00	20.00	20.00	40.00	50.00	50.00	μA

This chart pulls out from the data, those parameters having significant effect on inter-range compatibility. All devices operate with a positive supply voltage of nominally 5 volts and have similar *absolute maximum ratings* for supply and applied input voltages. The tabulated values apply only to active pullup output devices with inputs of unit load. Thus, flip-flops and other devices having inputs which represent two or more loads and also devices with open collector, resistive pull-up or buffer outputs, represent special cases.

NOISE IMMUNITY

Worst case D.C. noise immunity is a primary consideration and is defined as follows:-

D.C. noise immunity is the Difference between input threshold and input voltage applied using worst case values.

Thus: Low state Noise Immunity = $V_{IL} - V_{OL}$

High state Noise Immunity = $V_{OH} - V_{IH}$

A comparison across the range reveals the following results:-

	SN74L	SN74L*	SN74LS	SN74	SN74H	SN74S	
NOISE IMMUNITY VOLTS	0.4v 0.4v	0.4v 0.4v	0.3v 0.7v	0.4v 0.4v	0.4v 0.4v	0.3v 0.7v	(low state) (high state)

The worst case across the range is SN74LSN or SN74SN driving SN74L when low state noise immunity is 0.2V. (see table above).

These results indicate a favourable condition of overall noise immunity in a system employing products from all the ranges, bearing in mind that worst-case D.C. noise immunity is really a guarantee of worst case operation and typical noise immunities are closer to 1.0 volts for both low and high states.

Fan-out is the term used to describe the capability of our output to drive inputs. This is normally specified within a range and is guaranteed as follows:–

LOW STATE FAN-OUT = IOL ÷ IIL

HIGH STATE FAN-OUT = IOH ÷ IIH

This gives the results:–

		SN74L	SN73L*	SN74LS	SN74	SN74H	SN74S
FAN-OUT	LOW STATE	20	10	20	10	10	10
	HIGH STATE	20	20	20	10(20)	10	20

Thus the commercial ranges of SN74LN and SN74SN have a fan-out of 20 in the high state only. All recent devices in standard SN74N also provide a high state fan-out of 20 and where this becomes important the data sheet should be checked.

It is possible to derive fan-outs from range to range by using the simple formulae above and this together

with a rationalised approach to estimating System 74 inter-range fan-out is presented in the section on Loading and Compatibility.

This discussion on the technical aspects of System 74 has listed the product ranges initially offered. A comparison of the ranges from both an A.C. and a D.C. point of view has established that a philosophy of both horizontal and vertical selection of devices can offer the designer not only an effective increase of functions available, but also, the opportunity to optimise system design for speed and power dissipation.

Loading and Compatibility

LOADING AND COMPATIBILITY

In the previous section on the technical aspects of System 74 sufficient basic information is supplied to show that all the products offered share a similarity of characteristics allowing them to be used together. They are fully compatible.

The principal aim of this section is to demonstrate a method of inter-range Fan-Out computation that is simple, effective and allows optimal specification of each range. The argument is based on the SN74N ranges of TTL, but SN75N series Interface products can be considered as standard SN74N in that their designed capability to drive or be driven from TTL is parametrically based on standard SN74N.

Having demonstrated that the TTL ranges of SN74LN, SN74LSN, SN74HN, SN74N and SN74SN are completely compatible with regard to operating voltage levels, it becomes an elementary exercise to derive inter-range fan-out by respectively considering the current output capabilities of the different ranges and the input current requirements. The following matrix chart shows the result of calculating D.C. fanout across all the TTL ranges.

		DRIVING					
		74L	74L*	74LS	74	74H	74S
DRIVEN	74L	5	2.5	2.5	2.5	2.0	1.0
	74L*	20	10.0	10.0	5.0	4.0	4.0
	74LS	10	5.0	5.0	5.0	4.0	2.0
	74	40	20.0	20.0	10.0	8.0	8.0
	74H	50	25.0	25.0	12.5	10.0	10.0
	74S	50	25.0	25.0	12.5	10.0	10.0

SYSTEM 74 INPUT WEIGHTING CHART (STANDARD OUTPUT-UNIT LOAD)

Notes

1. This chart applies only to standard outputs driving unit load inputs. Buffer outputs, open-collecter outputs and resistive pull-up outputs are considered separately, as are greater than unity load inputs.
2. SN74L* includes half power versions of standard SN74 as identified by asterisks in the Selection Guide.

As stated, the fan-outs shown are calculated simply by considering the current parameters contained in the data sheets of each range. It should be noted that in most cases the fan-out is limited by the low-state output sink current. In other cases the fan-out is limited by the high-state output source current. Some examples of different cases are given.

	SN74L	SN74L*	SN74LS	SN74	SN74H	SN74S	UNITS
I_{OL}	4.0	8.0	8.0	16.0	20.0	20.0	mA
I_{OH}	−200	−400	−400	−400	−500	−1000	μA
I_{IH}	10.0	20.0	20.0	40.0	50.0	50.0	μA
I_{IL}	−0.18	−0.8	−0.36	−1.6	−2.0	−2.0	mA

SYSTEM 74 D.C. CURRENT PARAMETERS (STANDARD OUTPUT-UNIT LOAD)

EXAMPLE ONE

SN74 TO SN74L LOW STATE FANOUT IS $\frac{16\text{ mA}}{0.18\text{ mA}} = 88$

SN74 TO SN74L HIGH STATE FANOUT IS $\frac{400\text{ mA}}{10\text{ mA}} = 40$

LIMITING CASE IS HIGH STATE FANOUT OF 40

EXAMPLE TWO

SN74S TO SN74H LOW STATE FANOUT IS $\frac{20\text{ mA}}{2\text{ mA}} = 10$

SN74S to SN74H HIGH STATE FANOUT IS $\frac{1000\text{ mA}}{50\text{ mA}} = 20$

LIMITING CASE IS LOW STATE FANOUT OF 10

An appreciation of this mechanism is necessary. Where the high state fan-out is greater than the low state, it is permissible to connect unused inputs to used inputs since this has no effect on low state fan-out but does increase high state fan-out requirements. In fact SN74S, SN74L* devices and recently introduced SN74N products are specified to provide high state fan-outs of 20 and low state fan-outs of 10, specifically to deal with unused inputs. SN74L and SN74LS devices provide fan-outs of 20 in either state.

This derivation and charting of fanout rules provides useful information, but does leave a significant question unanswered. Where for example an SN74 output is driving a combination of inputs from some or all of the other ranges, the designer is still faced with the task of computing, in terms of input currents, the total loading effect. Thus, the fanout chart given is useful in computing the fan-out situation where the driven inputs are all from the same range. To improve the overall usefulness a normalising technique is applied to the fan-out chart.

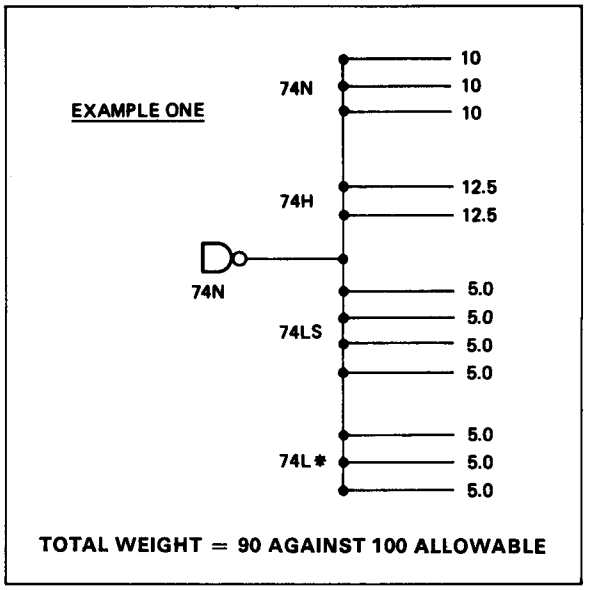
Divide all fan-out values into 100 provides the following Input Weighting Chart.

		DRIVING					
		74L	74L*	74LS	74	74H	74S
DRIVEN	74L	5	2.5	2.5	2.5	2.0	1.0
	74*	20	10.0	10.0	5.0	4.0	4.0
	74L*	10	5.0	5.0	5.0	4.0	2.0
	74	40	20.0	20.0	10.0	8.0	8.0
	74H	50	25.0	25.0	12.5	10.0	10.0
	74S	50	25.0	25.0	12.5	10.0	10.0

SYSTEM 74 INPUT WEIGHTING CHART (STANDARD OUTPUT-UNIT LOAD)

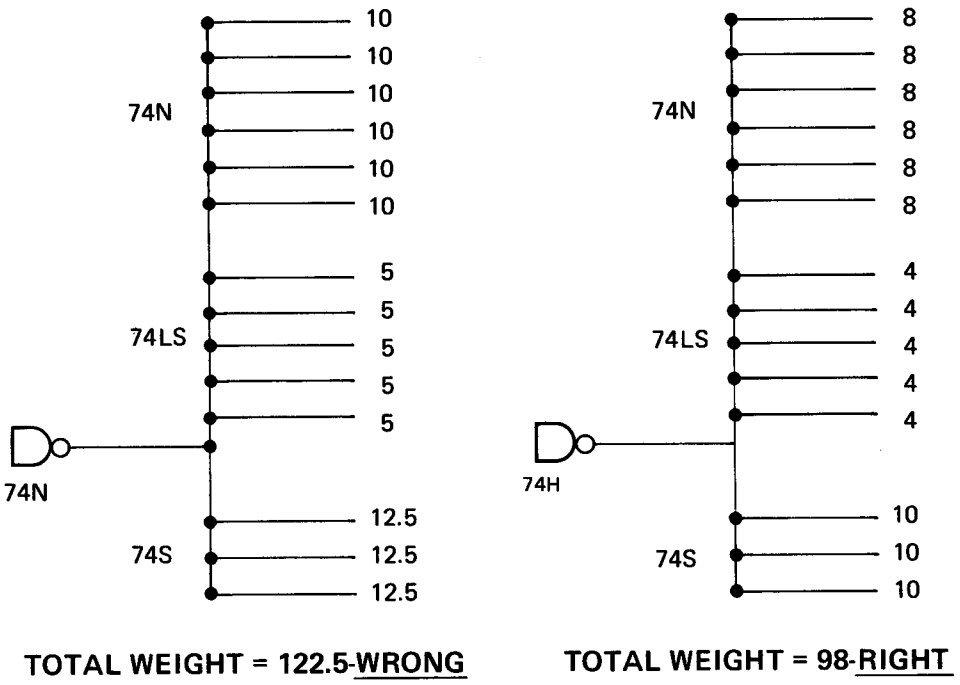
This variation of the fanout chart converts the fanout values to input weighting where the maximum weight applied to an output is one hundred. As shown the weight of a driven input is dependent on the type of driving output i.e. SN74L driven from SN74 has a weight of 2.5, or a weight of 2 when driven by SN74H.

Thus, to compute the loading effect of a combination of inputs simply add the appropriate input weight values. Up to one hundred represents a permissible loading, greater than one hundred will cause data sheet operating conditions to be exceeded.



In this case a complex loading situation is simply computed and found to be satisfactory.

EXAMPLE TWO



TOTAL WEIGHT = 122.5-WRONG **TOTAL WEIGHT = 98-RIGHT**

Here the loading requirement exceeded the permissible weighting but replacing the SN74N driving output with a more powerful SN74H device brought the loading to within that allowable.

Notes

1. The input weighting chart demonstrates the fact that System 74 allows very high fan-out situation. For instance a standard SN74S output can drive 100 SN74L inputs and thus simplify many design problems.
2. The input weighting chart is derived for standard outputs driving unit load inputs. However, its use can be simply extended to other situations. Thus, an SN74 buffer driver has three times the drive capability of a standard output and this allows the weighting to be increased to 300. This applies to all buffers with normal active pull-up outputs and thus an SN74S buffer can drive 300 low power inputs.
3. A certain number of System 74 products have input loading of greater than unity, i.e. flip-flops. In this case the input weighting is increased in proportion to the increase in input loading above unity.
   Thus, when driving the clock input of an SN74L flip flop from SN74, the input weighting shown on the chart should be increased from 5 to 10.

This system is derived from the data sheets, and they represent the most authoritative and complete source of design information. However, given an understanding of the derivation of this input weighting system, the designer has a valuable tool for quick evaluation of complex loading problems.

The most effective method for utilizing this sytem is to use it as a feasibility check. In the standard case where total allowable weighting is one hundred the following procedure is suggested:-

A RESULT OF UP TO 90 – NO PROBLEM

A RESULT OF BETWEEN 90 – 110 – CHECK AGAINST DATA

A RESULT OF OVER 110 – FIND ANOTHER SOLUTION.

The system can be extended to any situation where it is possible to derive a loading figure from the data sheets and can be simply modified to include SN75 series products, open collector TTL functions and pull-up resistors, by adding additional rows and columns. The designer can thus maintain flexibility by generating additional information and discarding that not required for a particular project thus keeping complexity and possibility of error to an acceptable minimum.

Use of TTL

USE OF TTL

System 74 is a very easy family of logic to use. With some types of logic there are many complications both from the logic design point of view and the system building. These add up to cost time and money before producing the final unit. Fan out calculations, the number of inputs that one gate can drive, can be different for almost every output, whereas, as seen it is very simple with System 74. The designer is also helped, more than many realise, by the multitude of complex functions which are standard catalogue items. It is no longer necessary to design an up/down counter from basic gates and flip flops. Such a function and others which are even more elaborate are now quite commonplace.

The ability to make sophisticated devices allows new techniques which would otherwise be unthinkable. An example is the use of ROM look up tables for multiplication. Another is the use of multiplexers instead of shift registers for parallel to serial conversion and vice versa. These new techniques can give a reduction in package numbers and apparent complexity.

Ambient temperature and supply voltage considerations are simpler with System 74. Due to the worse-case worse-case way in which System 74 devices are specified, provided they are nowhere outside the operating voltage and temperature ranges but no matter what the combination and distribution of voltage and temperature, then the devices will work correctly.

On top of this comes the safety margin which System 74 devices have. A typically series 74N output can sink about twice its guaranteed logical 'O' current of 16mA and still have an output voltage of less than 400mV.

Usually that output transistor will sink 40 or 50mA before it comes out of saturation. The logical '1' output current will typically be several milliamps giving an even greater safety factor.

As will have been seen there are few special considerations which need to be made. A brief look at the design of the logic and its testing will justify this.

Design Characteristics

System 74 TTL digital integrated circuit families optimize the advantages of saturated logic circuitry and monolithic semiconductor technology, yielding improved performance in the speed/power ranges which meet the needs of current and future designs. In other forms of logic circuitry (non-monolithic) maximum use is made of lower cost passive components (diodes and resistors) instead of higher performance (and higher cost) transistors. However, in monolithic circuitry it costs very little more to build transistors than diodes or resistors. Therefore, transistors are used to take advantage of the improved performance and also to buffer the fluctuations in currents that occur as resistor values change. The TTL multiple emitter input transistor replaces conventional input diodes, and an active pull-up output transistor eliminates the slow rise times associated with passive pull-up.

Each low-capacitance emitter of the input transistor offers very little loading to the driving circuit. In addition to providing some gain when this transistor is turned on (one or more emitters at a low voltage), a low impedance path (approximately $V_{CE(sat)}$) is established to remove the base charge from and turn off the phase-splitter transistor. When compared to a passive-component input, the TTL input is considerably faster.

Another important feature which reduces overall switching time of the TTL circuit is the active pull-up output. In addition to reducing the turn-off time, the double-ended output provides a low-impedance path in both the logical 0 and logical 1 states for sourcing or sinking current to highly capacitive loads and for rejecting capacitively-coupled a.c. noise.

A comparison of typical saturated digital logic family speed/power products is shown in Table A and Figure 1

Table A

Circuit	t_{pd}(ns)	P_T (mW)	Speed/ Power Product	Typical Fan-Out
74L TTL	33	1	33	10
74 TTL	10	10	100	10
74H TTL	6	23	138	10
DTL	25	5	125	8
DCTL	15	10	150	3
RCTL	30	10	300	4
RTL	50	10	500	4
74S	3	19	57	10
74LS	10	2	20	20
75	10	10	100	10

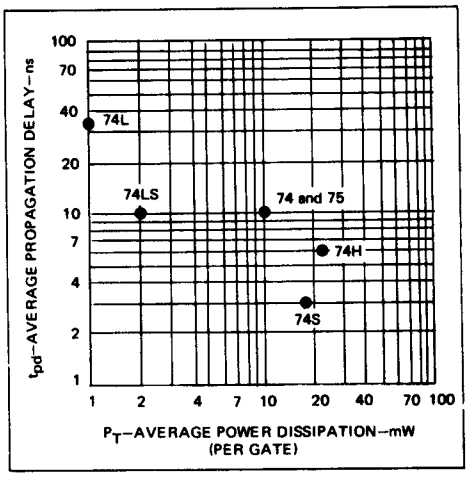


Figure 1.

Specification sheets can be misleading unless test conditions are clearly stated. One of the most important but least apparent benefits of System 74 TTL ICs is the guarantee that worst-case test conditions are used when specifications are prepared. The data sheets verify these worst case test conditions, including supply currents which are specified at maximum supply voltages.

Worst-Case Temperature

All d.c. limits shown on the data sheet are guaranteed over the entire temperature range of 0°C to 70°C. Texas Instruments guarantees one value over a temperature range since the designer is limited by whatever happens to be the worst value of a particular parameter regardless of the temperature at which it occurs.

Worst-Case Loading

For a logical one output voltage test, a guaranteed fan-out of ten is simulated by drawing at least ten times the current drawn by a worst-case input.

For example: 400 μA is drawn from the output of a Series 74N gate. Since an input at 2.4V can draw no more than 40 μA, the 400 μA drain represents a worst-case normalized fan-out of 10. Similarly, in the logical zero state, current equal to a worst-case fan-out of ten is "sunk" into the lower output transistor. See Figure 2.

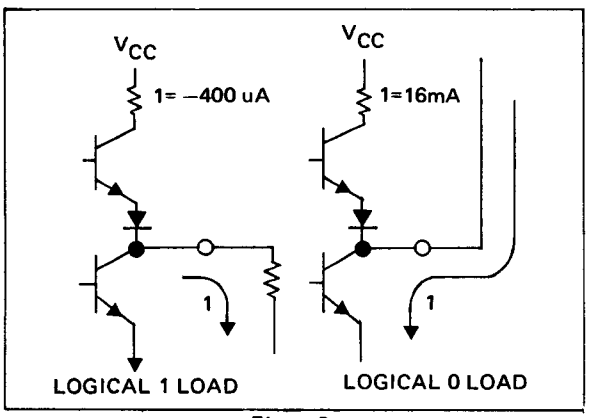


Figure 2.

Worst-Case Supply Voltage

The logical one output voltage follows changes in the supply voltage practically volt for volt; therefore, when measuring logical one output levels, the worst-case supply voltage is the lowest allowable.

Similarly, the low supply voltage limit is used when a logical zero output is tested since the lower voltage reduces the base drive to the output transistor and makes it more difficult to keep the transistor in saturation. See Figure 3.

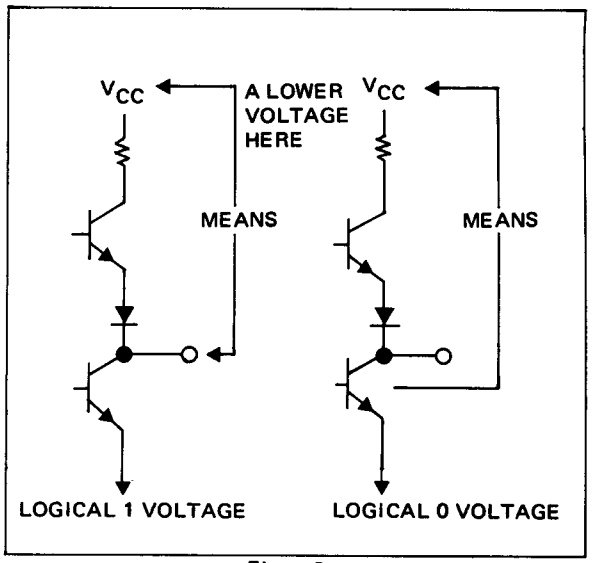


Figure 3.

Requirements are different, though, when an input is tested. Here, the high-limit power supply voltage is used, i.e. 5.25V, since the higher voltage results in more current into and out of the input. See Figure 4.

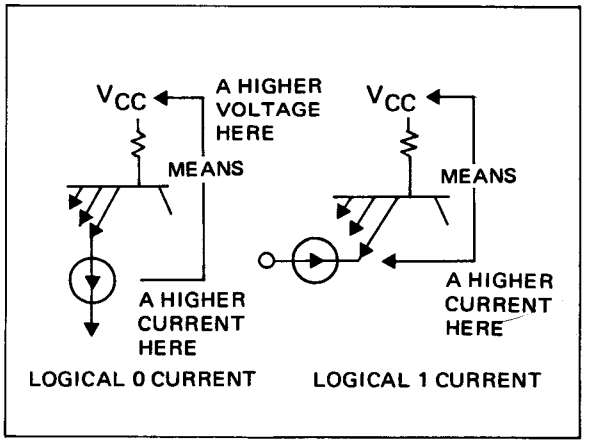


Figure 4.

These tests are extreme since supply voltages remain generally constant throughout any given system, but worst-case testing here gives added assurance of reliable system operation.

Worst-Case Conditions on Unused Inputs

In addition to selecting worst case supply voltages for various output conditions, worst-case voltages are also applied to the unused inputs as shown in the illustrations.

When a worst-case logical zero (0.8V) is applied to an input and where that voltage is required to hold the output transistor Q in the off state – unused inputs are returned to the maximum supply voltage. This represents the worst-case condition since these high voltages would tend to turn on the transistor Q if it were not for the low input. See Figure 5.

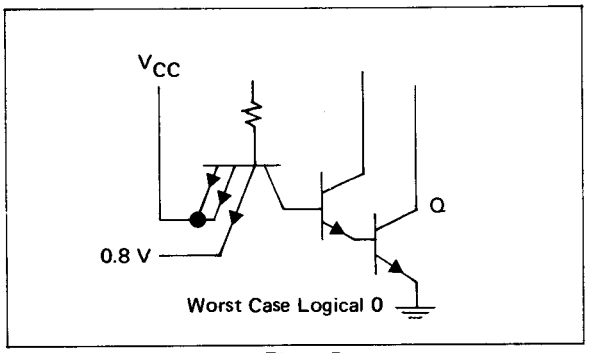


Figure 5.

When a minimum logical one (2.0V) is applied to an input to turn on the output transistor Q, the worst case is to hold all other inputs at the minimum logical one voltage which is 2.0V. Therefore, all inputs are tied together and taken to this voltage. See Figure 6.

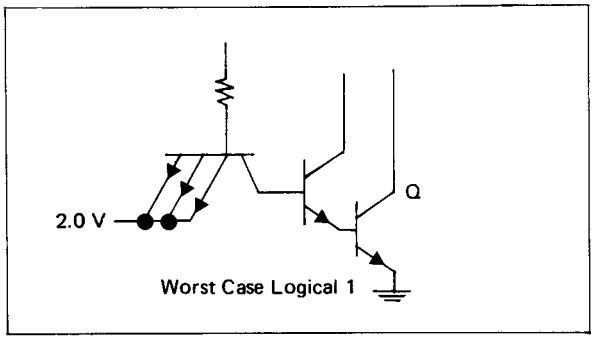


Figure 6.

Worst-Case Supply Current

Power supply current requirements for all System 74 TTL circuits are specified as maximum current drains with power-supply voltage at V_{CC} = MAX. When power supply currents are specified at the nominal V_{CC} (5 volts), the true worst-case current drain is not obtained. I_{CC} at nominal V_{CC} is, in fact, approximately 91% of the worst-case value, and the resulting power dissipation is approximately 82% of the worst-case value.

In summary, worst-case testing of every parameter may result in figures that look less impressive than those obtained with more typical testing, but it gives you extra assurance that every circuit will perform correctly in your system, under worst-case conditions.

With a linear system it is possible to very simply measure the performance and accuracy. A digital system however either works correctly or has faults. It is difficult to tell how near equipment is to malfunctioning. Although it has been said that there are few things to take into special consideration, there are simple guidelines which enable the best to be obtained from a system.

These general guidelines will be covered in the next few pages. Idiosyncrasies and features of individual devices will be discussed in the Applications Sections.

Power Supply

The supply voltage can be between 4.75V and 5.25V. Also different parts of the system do not have to be at the same voltage, provided it is never outside the above limits. As well as regulation only having to be 5%, ripply can also be up to 5%.

One of the things to bear in mind about power supplies for TTL systems is that not only must they cope with power consumption of the TTL circuits and any external resistors, but they must also be able to handle circuit switching transients and system capacitance at the designed operating frequency. Consider a simple TTL gate with a load capacitance C_L.

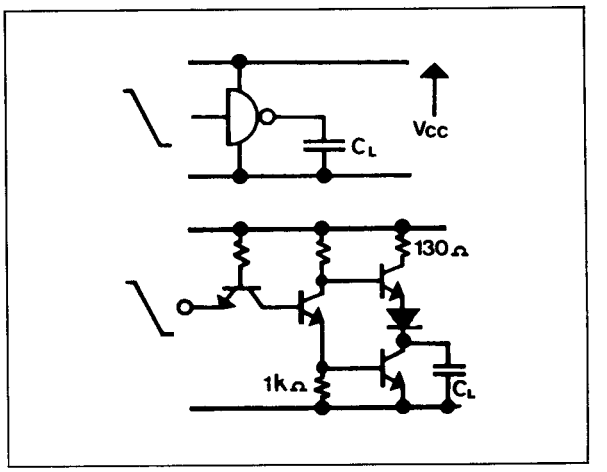


Figure 7.

When the input to the gate goes low there comes a point in the transition when the upper transistor in the totem pole output turns on, while the lower output transistor is still in the process of turning off due to the stored charge in the base/collector junction, discharged through the 1kΩ resistor. As a result there is a brief period in time during the transition when both output transistors are on.

Now the dynamics of the switching and internal feedback are such that this condition only lasts for about 7ns with 74N Series TTL. The maximum current which flows down the output is not so much governed by the 130 ohm resistor (which would allow up to 25mA) but rather by the switching dynamics, and it is in fact about 8mA max. One can illustrate the current drawn by the circuit when switching as below.

The charge represented by the current spike is independent of frequency and input rise and fall times (so long as these are submicrosecond) and is about 30. 10^{-12} coulombs. As the frequency rises these small spikes start to contribute to the average I_{CC} current. A graph below shows this. At 10 MHz for instance, $I_{CC} = 10^7 \times 30 \times 10^{-12}$ amps = 0.3mA. Thus I_{CC} (total) = 2.3mA = I_{CC} (DC) + 15%.

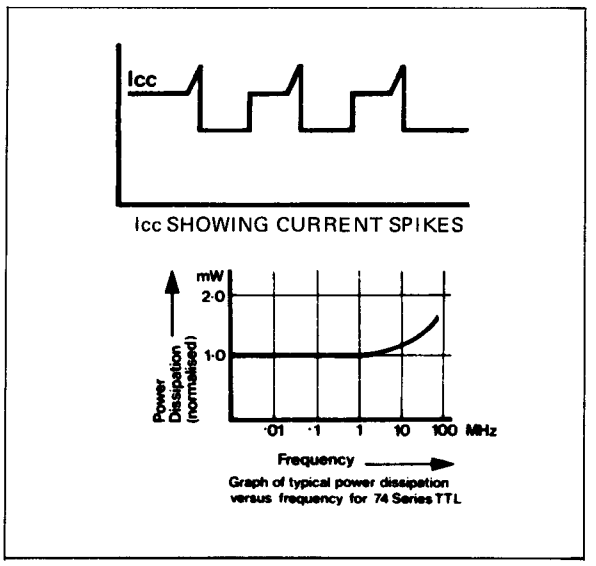


Figure 8

Now one of the other factors one should consider is the charge/discharge of load capacitance C_L, typically 15pF in a system with short lead lengths. C_L is charged from about 0.3 volts to 3.3 volts each cycle, which represents $15 \times 10^{-12} \times 3 = 45 \times 10^{-12}$ coulombs. At 10MHz this can be expressed as follows.

I_{CC} (capacitance) = $10^7 \times 45 \times 10^{-12} = 0.45$mA.

$\therefore$ I_{CC} (total) = I_{CC} (DC) + I_{CC} (transient) + I_{CC} (capacitance)

= 2.0 + 0.3 + 0.45 = 2.75mA.

This is a typical figure for a gate circuit.

The increased system current required at 10MHz can be directly related to the number of output nodes in the system by adding the DC current to 0.75mA x the number of nodes.

From these considerations, it is possible to determine the size of power supply required. One can then arrange for the supply to have sufficient regulation and stability. Even with the best regulation some mains-borne noise can propagate through the regulator. In severe cases, R.F. filter the primary of the transformer and use one wound with an electrostatic screen.

Decoupling

Decoupling should be distributed on the board with 0.1 μF ceramic capacitors for every 5 to 10 packages. These are designed to decouple high frequency noise which the logic, being fast, is capable of propagating. They must therefore be connected across the V_{CC} and ground lines (that go to the *same* package) by short leads and good R.F. practice. The actual power supply, which may claim to be a low impedance, will cease to be so at frequencies above a few kilohertz. Therefore earth planes and broad tracks with decoupling are necessary to give a low impedance supply at the device.

Grounding

Care should be taken with the construction and layout of the logic. System 74 is fast (it has fast edges), even the low power devices. Therefore some consideration must be given to the way gates are put together. A ground plane is desirable. It can also have the V_{CC} track on the same side of the p.c.b., if it is wide and decoupled well. If this physically cannot be done, then the earth and supply rails should be as broad as possible wherever possible.

In terms of inductance, it is advantageous to parallel tracks. Paralleling two tracks is much better than doubling the width of a narrow track.

Data rise and fall times into TTL devices should be 50ns except in the case of Schmitt triggers.

If the edges are not this fast then it is possible for a gate to be affected by noise or feedback as the input voltage is at the threshold. The effect looks like a burst of oscillation as the gate output switches from one state to the other. This can of course affect bistable elements such as counters giving an apparent random change in the outputs. Slow edges usually come from input signals (or deliberate time constant circuits which should thus be avoided). Schmitt trigger gates ('13, '14 and '132), as will be seen, can be used to advantage here.

Unused inputs of ALL TTL devices should be tied to guaranteed logic levels.

An input left open circuit on the bench will act as a logical '1' input. In practise this should definitely not be done. Again it can be connected to V_{CC} but this should be done with caution.

One of the first things to remember is that even the most stable power supplies can have transients. In most industrial applications these days it is usual to see considerable coupling of external noise sources (controllers, motors, contactors, etc.) into power supply distributions in logic systems.

It is unwise to tie up unused inputs to V_{CC} since in most environments it is difficult to maintain power supplies within the 5.5 volt rating demanded by this. There are four alternatives:

1. Leave them open circuit.
2. Tie them to V_{CC} through a current limiting resistor.
3. Tie them to the output of an unused gate held in the one state.
4. Common them with another input on the same gate and drive them.

Whilst "1" is satisfactory for gates, it slows down propagation delay because the capacitance to ground associated with the input (bond wire, package pin, etc. approx. 1.5pF) adds an extra time constant in the $t_{pd(o)}$ equivalent to about 1.0 ns.

Data inputs to flip-flops and counters should always be tied somewhere, and preset/clear lines MUST be tied to a voltage. This is because of high regeneration from preset/clear lines which causes latching to occur for much lower levels of noise energy.

"2" is satisfactory, but requires an external component. The value of the resistor should be a minimum of 750Ω. The capacitance-to-ground time constant is eliminated, but there is still emitter-emitter capacitance accounting for approximately 0.5 ns delay in $t_{pd(o)}$.

"3" is a very good method since unused inputs are then in the same environment as driven inputs, i.e. a low impedance system (Z. out (1) ≈ 100Ω) with two diodes up to V_{CC} for over-voltage protection. Speed is the same as "2".

"4". If there is spare fan-out capability in the system, commoning up inputs results in optimum speeds, since all stray capacitance associated with inputs is being driven from low impedance. For the purposes of fan-out computation, two inputs paralleled (on the same gate) have a fan-in of 1 in the zero state, and may be taken as 1.5 in the high state. System 74 TTL has, in many cases, a fan-out of 10 in the low state, and 20 in the high state, allowing extensive commoning of inputs for optimum speed.

Summarizing:

Do not, if possible, tie spare inputs to V_{CC}.

Do not, if possible, leave gate inputs floating.

Do not, if at all possible, leave date inputs floating.

NEVER leave preset or clear lines floating.

In small to medium systems, try to tie unused inputs to a spare gate held in the one state – if this is not possible, use a resistor to V_{CC}. In large systems, drive all spare inputs for optimum speeds.

INPUT RATINGS

Positive Rating

The date sheets guarantee a 5.5 volt rating on inputs with a 1mA current maximum. Essentially this guarantees a breakdown condition on the input rather than a leakage current, and TI test for the worst case configuration with other inputs at earth.

In this way TI guarantee the base emitter breakdown voltage of the input under test and include the effect of all the currents flowing as a result of the emitter – emitter gain in the multi-emitter transistor. The base of the transistor sits a V_{BE} above earth, and therefore the actual junction breakdown is guaranteed at 5.5 – V_{BE} = 4.8 volts.

When driving the input from another TTL gate in the one state, the driven input sees about 100 ohms in series with two diodes as shown below.

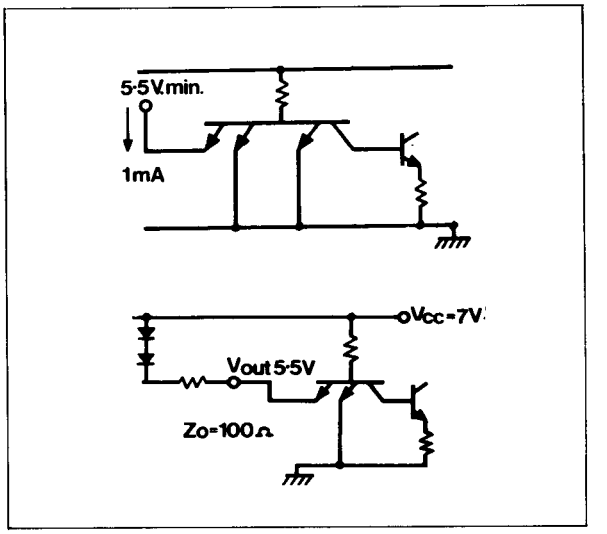


Figure 9

When V_{CC} rises above the recommended operating limits of 5.25 to 7 volts – the maximum rating for System 74 devices – the V_{out} of the driving gate rises to about 1.5 volts below V_{CC}, i.e. 5.5 volts which represents the DC rating of the following gates' input.

So when you're driving into TTL from any device with a resistive pull up to V_{CC}, there's no V_{BE} limiting like we have in the TTL stage outlined above, and in these circumstances you must define a minimum value for resistor R to limit the breakdown current which will flow into the TTL input under V_{CC} fault conditions. We recommend a minimum value for this resistor of 750 ohms. This limits the maximum breakdown current in any input to 2mA which is a safe value to use as a DC rating.

If you need a lower value resistor (for instance to increase the wired AND capability of open collector TTL devices) then you can make use of the higher breakdown voltage obtained if other inputs are not at earth, but tied together.

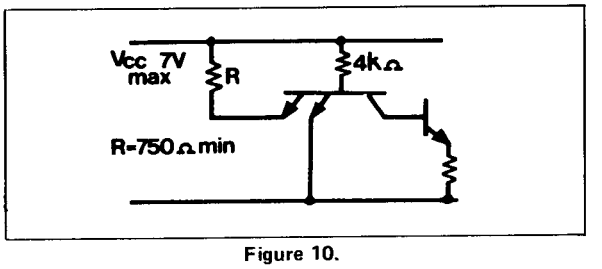


Figure 10.

The base of the multi-emitter transistor will now sit at 2.1 volts and the breakdown voltage seen at the emitters will be 4.8 + 2.1 = 6.9 volts. And only a nominal current limiting resistor, R, of 100 ohms is needed for a maximum V_{CC} rating of 7 volts. This gives plenty of scope for a wide wired AND application. In all cases it is preferable to use the highest value resistor possible up to 1 kilohm, consistent, of course, with the application.

Negative transients caused by switching on transmission lines are well within the device rating, so they are no problem. However, DC ratings are governed by a current or a voltage limit, whichever is the more stringent, and they are defined as follows:

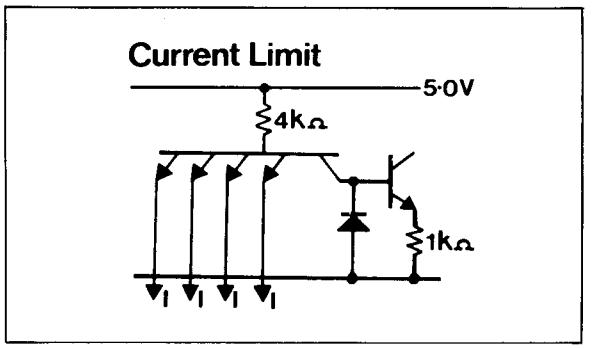


Figure 11.

The current above is drawn from the substrate via the collector isolation diode shown – 1 = 5mA per input maximum or 25mA total, whichever is smaller.

Now for voltages, the limit in the configuration shown below is limited by the 5.5 volt emitter – emitter DC breakdown condition, and therefore the maximum negative voltage guaranteed on the inputs is –2.2 volts.

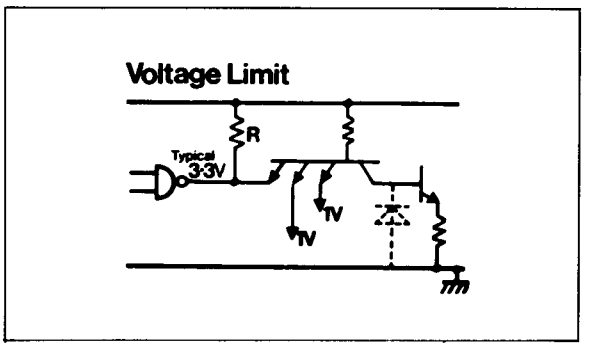


Figure 12.

As with positive voltages greater than 5.5 volts, there is also a limit with negative voltages above the 5.5 volt rating, and a maximum current limit of 2mA must be observed into any input.

Consider the circuit below. Here the maximum negative value for V is given by I_{max} = 2mA (DC rating), so where V = –2.2 volts maximum this gives R_{min} = 850 ohms with a nominal V_{CC} of 5.0 volts.

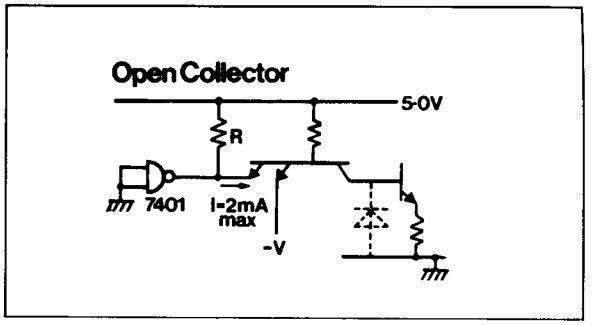


Figure 13.

It is not recommended to use System 74 devices with inputs taken to negative voltages. However, if this is really necessary, one can make use of the increased negative voltage rating available by driving all the inputs together as shown in the circuit below.

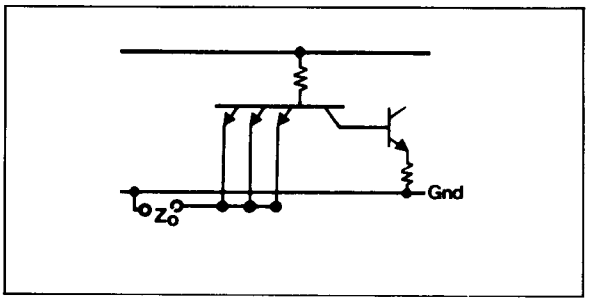


Figure 14.

In this way no emitter breakdown can occur and it ensures that the Z_0 of the source is sufficient to limit the current to 5 mA per input (one can safely assume equal current sharing).

Increased fan out can be obtained by paralleling devices in the same package.

Gate expanders should lie as close as possible to the gate being expanded. This avoids capacitive loading and noise pick-up.

Input date to master slave JK flip flops should not be changed when the clock is high.

NOISE IMMUNITY

Noise immunity is a vital consideration when evaluating integrated circuits since noise can, under certain conditions, falsely trigger gates and introduce errors into the system.

First consider the effect of noise on the individual device.

a-c or d-c noise

It is difficult to define a-c noise and even more difficult to relate it to a specification. Generally, d-c noise is worst case. When noise immunity is plotted against pulse width, it can be shown that the circuit is more immune to noise as pulse width decreases. See Figure 15.

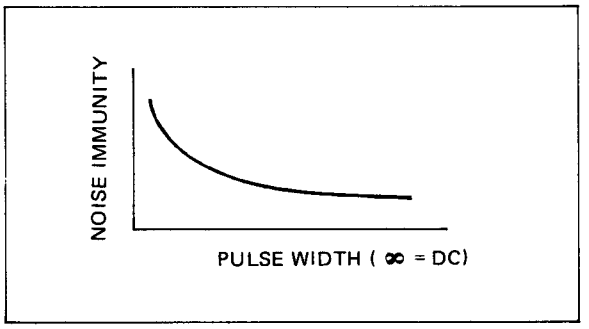


Figure 15.

Susceptibility

When discussing a-c noise, the term "noise susceptibility" is more appropriate than "noise immunity".

Low logical one a-c noise susceptibility

An important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12Ω and logical 1 output impedance is 70Ω for standard Series 74N circuits. See Figure 16. This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R–C time constants which preserve waveshape integrity.

This means a-c noise susceptibility is far better than logic circuits which have 2000-ohm logical one output impedances.

As a result, System 74 TTL is much more effective than other forms of logic at preventing noise from ever appearing at the output. In addition, it has high immunity to d-c noise from supply voltage and ground sources.

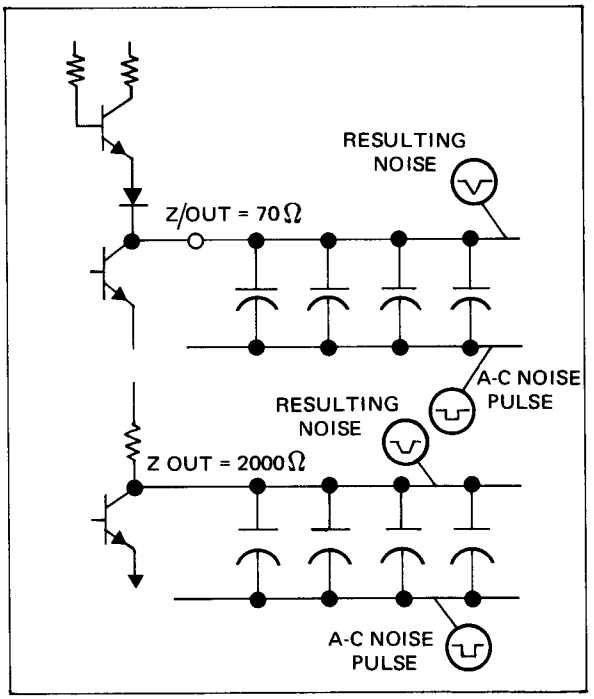


Figure 16.

Supply Voltage Noise

Notice that the output of a System 74 gate, Figure 17, is similar to an emitter-follower circuit. For loads even considerably higher than fan-outs of ten, the transistor Q_1 does not saturate when the gate is in the logical one state. Therefore:

$$V_{OUT} = V_{CC} - IR - V_{BE(Q_1)} - V_D$$

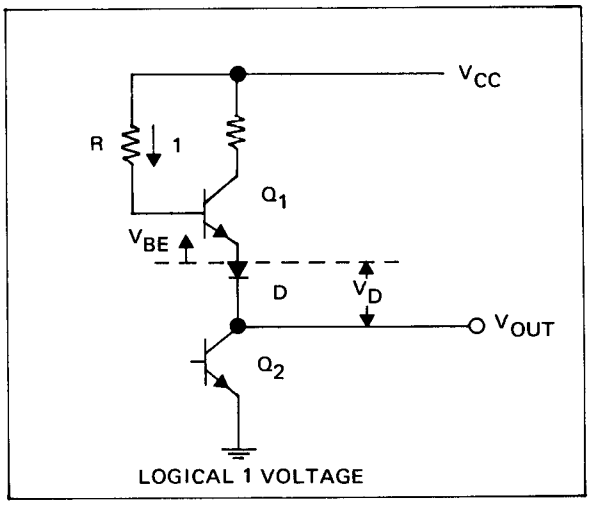


Figure 17.

As the voltage changes across the resistor R, the base emitter junction of Q_1, and the diode are small, the output voltage follows the supply voltage very closely in the logical one stage. A negative voltage change on the supply line is reflected almost directly to the signal output line.

The high logical one d-c noise immunity reduces the probability of false triggering due to supply voltage variation.

Ground line noise

In the logical zero state, Q_2 saturates and a positive transistion on the ground line is seen on the signal line.

Therefore, both supply voltage noise and ground line noise appear as signal line noise. Thus, the treatment of d-c noise can be discussed comprehensively by concentrating on the signal line only.

Typical d-c noise immunity

System 74 gates change state as the changing input voltage passes through an approximate 1.4 volt threshold. The output is typically 3.3 volts in the

logical one state (see Figure 18) and 0.2 volt in the logical zero state. Therefore, the output can typically tolerate 1.9 volts of negative-going noise in the one state and 1.2 volts of positive-going noise in the zero state before causing the gate it is driving to falsely trigger. In both states, System 74 has more than one volt typical noise immunity. See Figure 19.

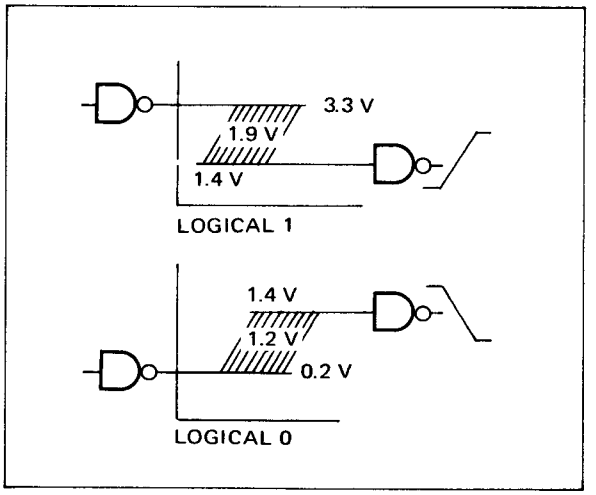


Figure 18.

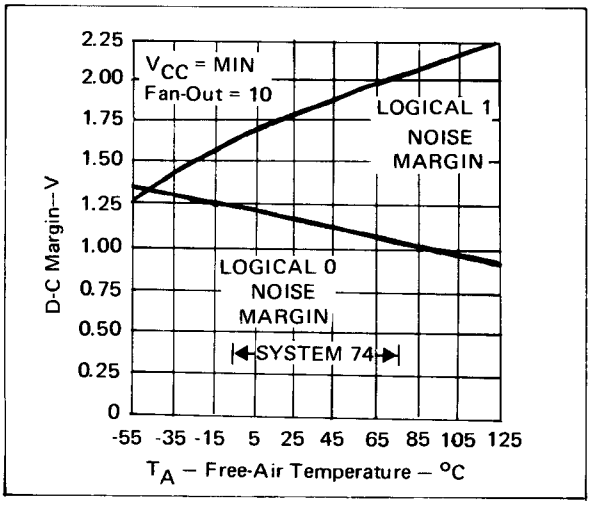


Figure 19.

Guaranteed d-c noise immunity

Simply stating that a circuit will not falsely trigger is not an adequate guarantee for a design engineer. The manufacturer must also guarantee an absolute output voltage limit which will not be exceeded when noise is applied to an input. Figure 20 shows these guaranteed voltages.

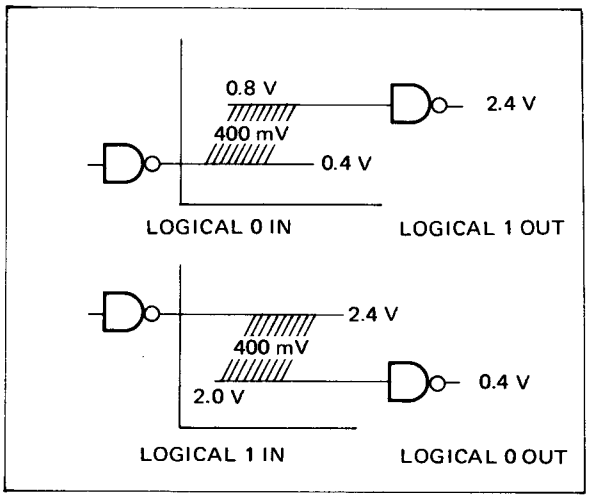


Figure 20.

The logical zero input test voltage is 0.8 volt, and TI guarantees a maximum logical zero output of 0.4 volt which gives a guaranteed noise immunity of 400 millivolts.

Likewise, the logical one input test condition is 2.0 volts which is 0.4 volt below the guaranteed minimum logical one output of 2.4 volts.

In both states, guaranteed noise immunity is 400 millivolts.

Having seen what noise immunity is inherent in the device design now consider the noise immunity of a system and how it can be simply improved.

Noise considerations in digital systems may be summarised as shown in Figure 21.

Each topic shown cannot be considered in isolation, but must take into consideration the influence of other factors, for example, internal noise only becomes important if it is significant compared with data levels.

Internal Noise Generation

High frequency signal components due to fast transition times at the outputs of logic elements are the main source of internally generated noise. These components are still present when data rates are low, demanding that high frequency techniques should be used no matter what the pulse repetition rate.

As device logic levels change, circuit currents flowing also change. These changes are due to:-

(i) Different currents required to maintain the new logic level.

(ii) Transients due to lines charging and discharging.

(iii) Conduction overlap of the transistors in a TTL output stage.

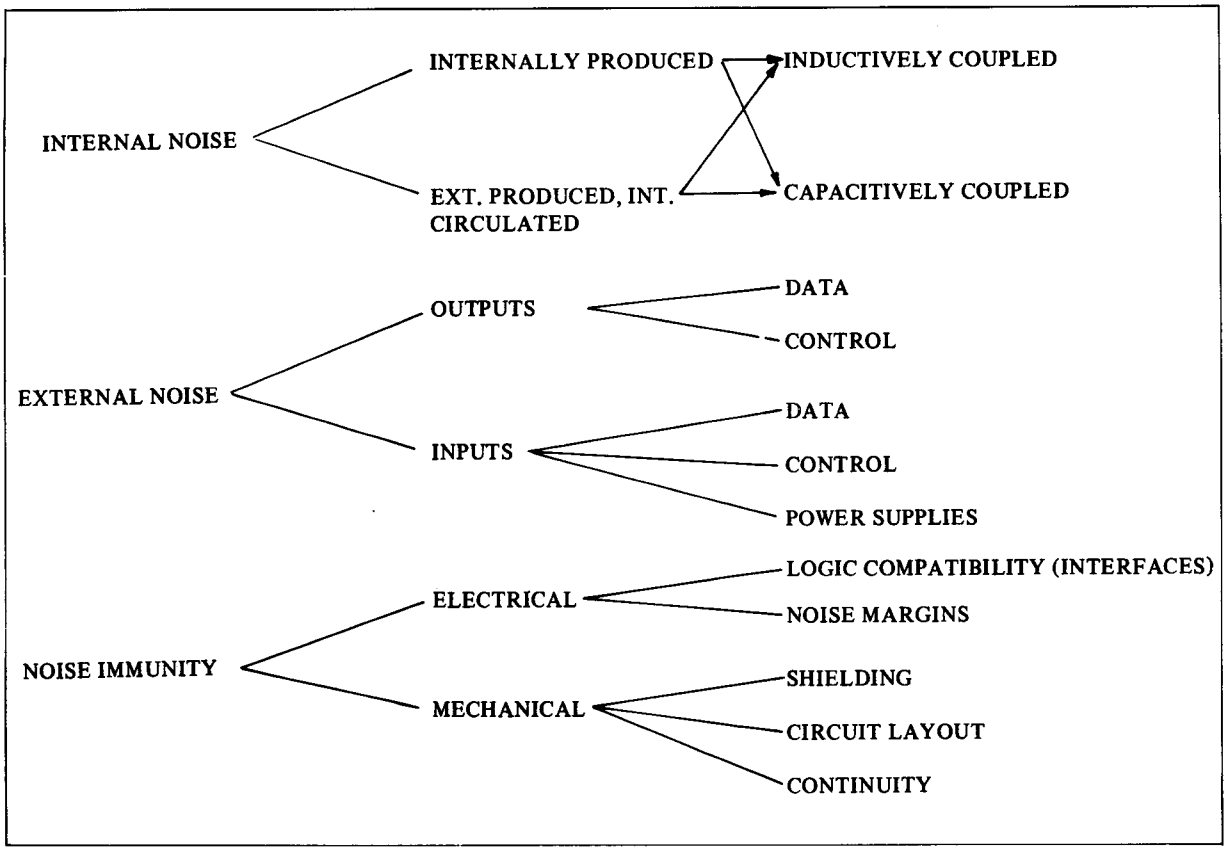


Figure 21.

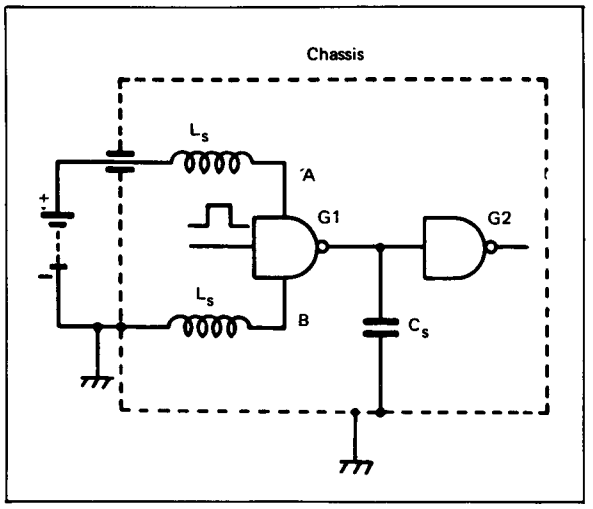


Figure 22.

Figure 22 shows the stray circuit elements associated with these transients.

Capacitance C_s is the capacitance to ground the surroundings of the output connection from gate G1 to the input of gate G2. L_s and L_g are the self inductances of the ground and supply lines respectively.

When the gate output changes from a logical '0' to a logical '1' capacitance C_s must be charged through inductance L_s from the supply. The charging current I_s being C_s. V/t_r, where V is the voltage difference between the logical '1' and '0' levels and t_r is the voltage rise time at the gate output. For standard TTL with typical rise and fall times of 7 ns or less, interconnection charging currents can be greater than 8mA per output. This together with conduction overlap in the output stage indicates that care should be taken with system layout so as to minimise supply line impedance and interconnection inductance.

In a practical system the following steps should be taken to minimise the generation of internal noise.

(i) The power supply distribution system should be of low impedance.
This can be achieved by two methods:

(a) A low impedance transmission line formed by a stripline above a ground plane – or line.

(b) Medium impedance line with decoupling to ground at regular intervals by discrete R.F. capacitors, e.g. disc ceramics. Decoupling should be carried out every 8 to 10 packages. Use 0.01 μF to 0.1 μF or 200pF per totem pole output, whichever is the greater value. These should be distributed throughout the circuit, not lumped together. Both ends of a long ground bus-bar should be returned to a common point.

(ii) Gates that drive lines must be decoupled at the package. The decoupling capacitor and transmission line ground should be commoned as near to the driving device ground as is practical.

(iii) Power gates formed by paralleling gates should utilise a single package with its decoupling capacitor.

Noise that has gained entry to equipment as well as that which is internally generated can couple into adjacent signal and power lines. This can take place through common impedances or as shown in Figure 23.

Here two lines carrying signals, or signal and noise, are in close proximity to one another. Cross coupling exists between these two lines due to mutual capacitance and inductance C_m and L_m. In order to analyse this configuration, it is convenient to consider C_m and L_m forming a mutual impedance Z_m between the two lines. If the line impedances are Z_o, the gate output impedances are Z_1, the logic swing at the output of gate G1 is V_s, and the coupled component of V_s at the input of G4 is V_{in}.

$$V_{in} = V_s/(1.5 + Z_m/Z_o)(1 + Z_1/Z_0) \ldots\ldots 1$$

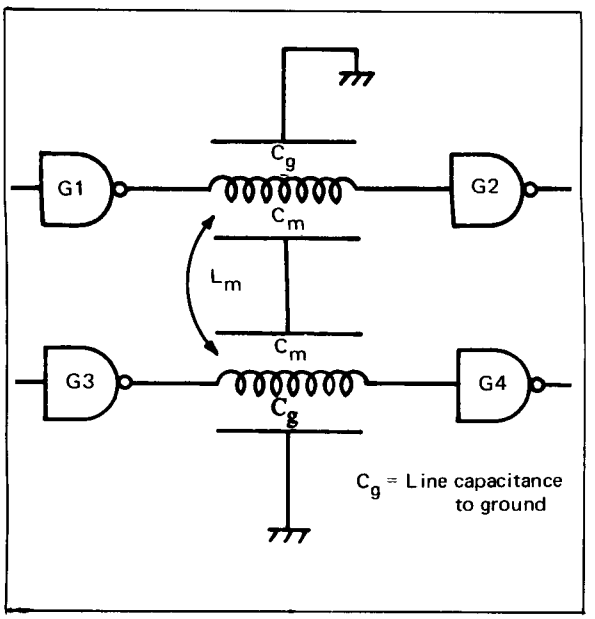


Figure 23.

The following practical conclusions can be drawn from equation 1.

1. To minimise cross talk between two lines their mutual impedance should be as high as possible and the line impedance as low as possible.
2. Such lines should be coaxial cables with low impedances Z_o and very little external field giving a high Z_m.

In practice the line impedance cannot be too low or the logic swing at the receiving gate will be restricted and line reflections will be significant compared with logic levels.

Stripline conductors above a ground plane can have controlled impedances giving excellent crosstalk properties.

Single wires, whilst being inexpensive and convenient, have poor cross-talk and reflection characteristics limiting their usable length to 25cm or less with standard TTL.

For lines less than 5m in length twisted pairs with Z_o between 50Ω and 150Ω are satisfactory provided that the sending gate is restricted to line driving. (This is explained in more detail in the section on driving transmission lines.)

External Noise

In any digital system provision must be made for the transmission of input and output data and control signals between the logic system and its peripherals. The current and voltage levels chosen for transmission are generally incompatible with TTL as they are dictated by considerations such as line impedance, noise environment, contact resistance, etc.

The influence of external noise on a TTL logic system is determined mainly by the type of interface circuits used to transfer signals into the logic system. These circuits cannot be designed effectively unless the input requirements of a TTL gate are understood.

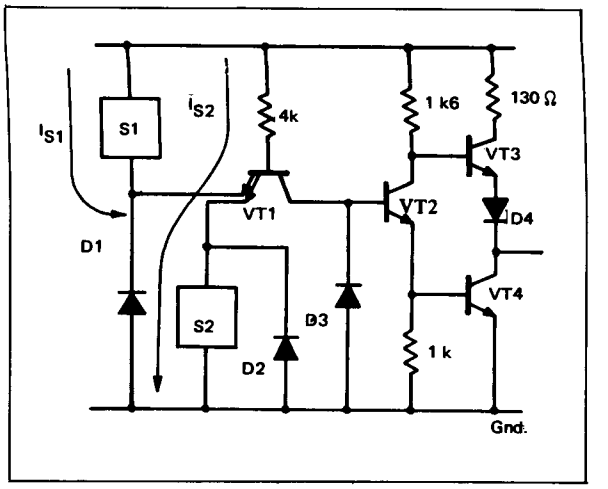


Figure 24.

Figure 24 shows the circuit diagram of a standard 74N series gate, where I_{S1} is the current to be 'sourced' and I_{S2} to be 'sunk' by the driver circuits S1 and S2.

Transistor VT1 is a multiemitter transistor with a 4kΩ base resistor to the supply voltage V_{CC}. If any input emitter is grounded base current flows out of the grounded emitter saturating transistor VT1 and turning 'off' transistor VT2 allowing its collector to

rise towards V_{CC}. The output of emitter follower transistor VT3 is, therefore, a logical '1'. If all input emitters of VT1 are high, i.e. logical '1' then its base collector diode is forwarded biassed and transistors VT2 and VT4 are saturated. The collector of VT4 is therefore at $V_{CE(sat)}$, i.e. logical '0'. Since the input transistor is now operating in an inverse mode with the collector to base diode forward biassed, an inverse emitter current, dependent upon inverse gain and base current, must flow into each emitter. The input voltage at which VT1 changes from normal to inverse mode of operation, i.e. the gate threshold voltage, is determined by its collector potential. This is defined by the V_{BE}'s of VT2 and VT4, giving a typical threshold of 1.4V.

A typical transfer characteristic of the circuit of Figure 24 is shown in Figure 25.

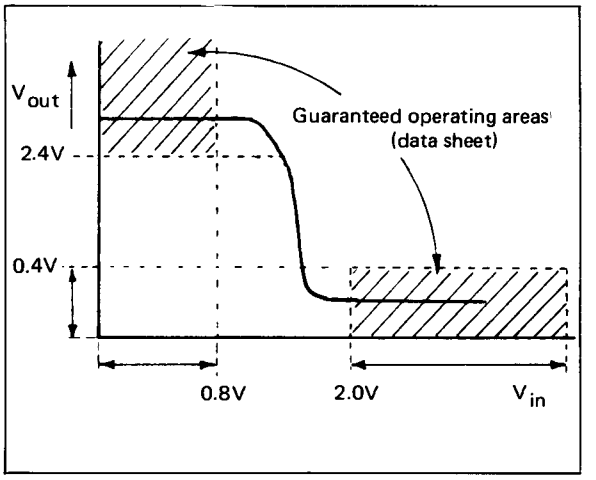


Figure 25.

To obtain maximum noise immunity logical '0' and '1' input levels should be far removed from the gate threshold. This means that any interface circuit must be able to sink base current of VT1 when in the logical '0' state and source the inverse emitter current when in the logical '1' state in order to maintain maximum noise immunity.

Interface Circuits

An interface circuit must perform the following operations:-

(i) Transform input logic levels to those of TTL. This must be achieved without loss of noise margin.

(ii) Filter out unwanted noise whose frequency components lie outside the signal frequency range. Noise that occurs within the signal frequency spectrum, i.e. comparable with data bit rate, can only be removed by logical means.

(iii) The interface circuit must take into consideration the transfer characteristics of the circuit that it is driving. The basic TTL gate is a saturating amplifier with a range of input voltages around its threshold where the gate will act as a high gain (>55dB power gain at 10MHz) high frequency linear amplifier.

The rise and fall times of data edges into TTL required for oscillation-free switching, are dependent upon a number of factors. These include the driving source impedance, gate loading, layout and supply decoupling. In practice, interface circuits should have rise and fall times (10–90%) <50 ns between logical '0' and '1' levels.

Input Interfacing

Figure 26a shows one of the simplest ways of connecting into TTL.

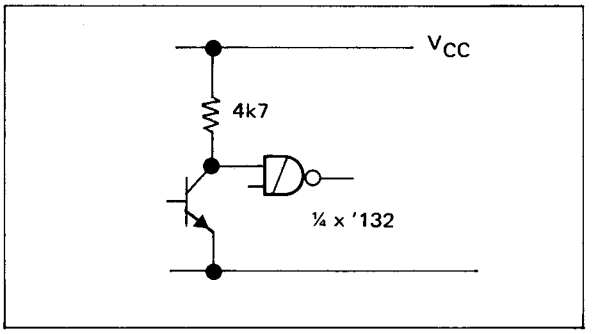


Figure 26a.

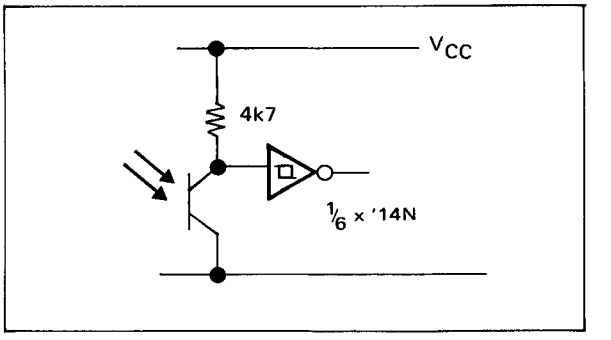


Figure 26b.

The transistor, when switched on and saturated, sinks the input current of the gate and when the transistor is off the gate input current which is then very small is provided by the resistor. Ideally, the gate should be a Schmitt trigger such as the '132N, to avoid oscillation and noise problems when the input voltage is around 1.5V. (A phototransistor can also be interfaced by this scheme as in Figure 26b).

Another well tried method where the inputs are driven by a low impedance such as a switch, uses a pair of gates across coupled as a latch, as shown in Figure 27. This arrangement can reduce the problems of switch bounce without needing a time constant.

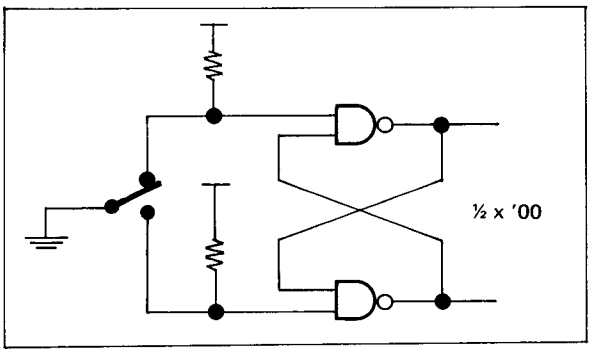


Figure 27.

A transistor, as in Figure 28, allows interfacing with high impedances, although with this simple arrangement the threshold will be at only 0.7 of a volt. There is therefore less than 0.7V noise immunity.

In most systems it is advantageous to have higher thresholds in order to overcome voltage drops down lines and contact resistance etc. Such circuits which have thresholds of about 12V are shown in Figures 28 and 29.

Both circuits consist of CR low pass filters followed by a transistor buffer and a Schmitt trigger. Capacitor C1 is a lead through ceramic. This, together with L (lead inductance), forms a low pass filter removing high frequency components that would otherwise, due to layout, be very difficult to remove. The logic threshold for the circuit of Figure 28 is arranged to be 12V midway between the input logic levels, 0 and 24V. The values of C1, C2 and C3 should be chosen to give the required frequency response.

Both circuits have a series resistor between capacitor C3 and transistor VT1. This limits the rate of discharge of C3 through the base emitter diode of transistor VT1.

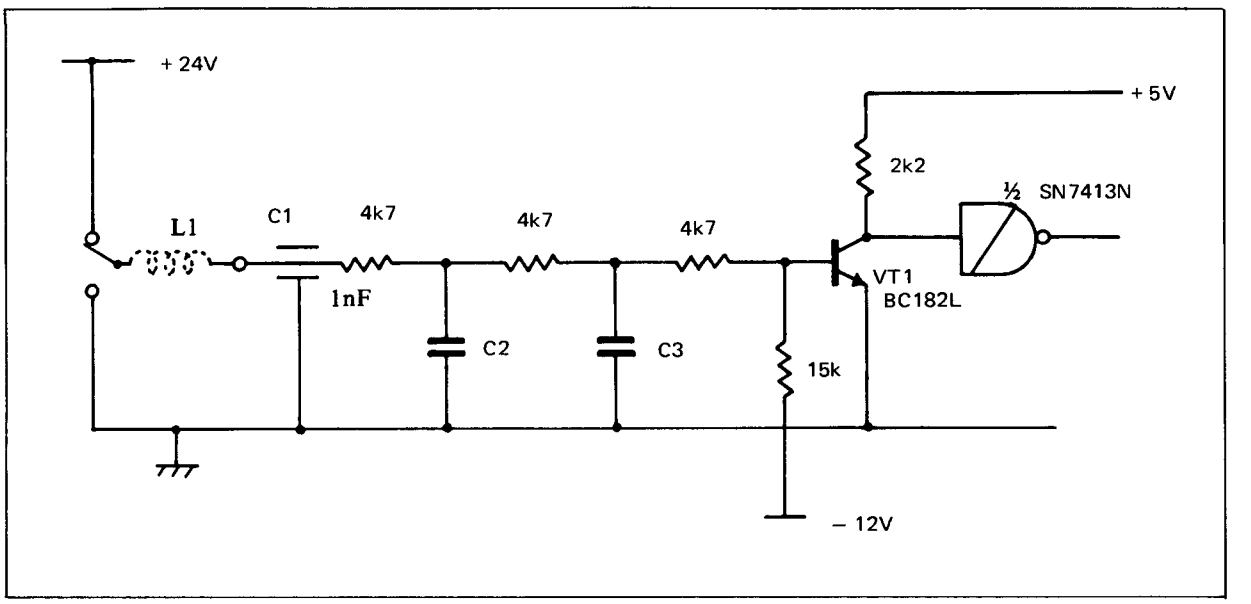


Figure 28.

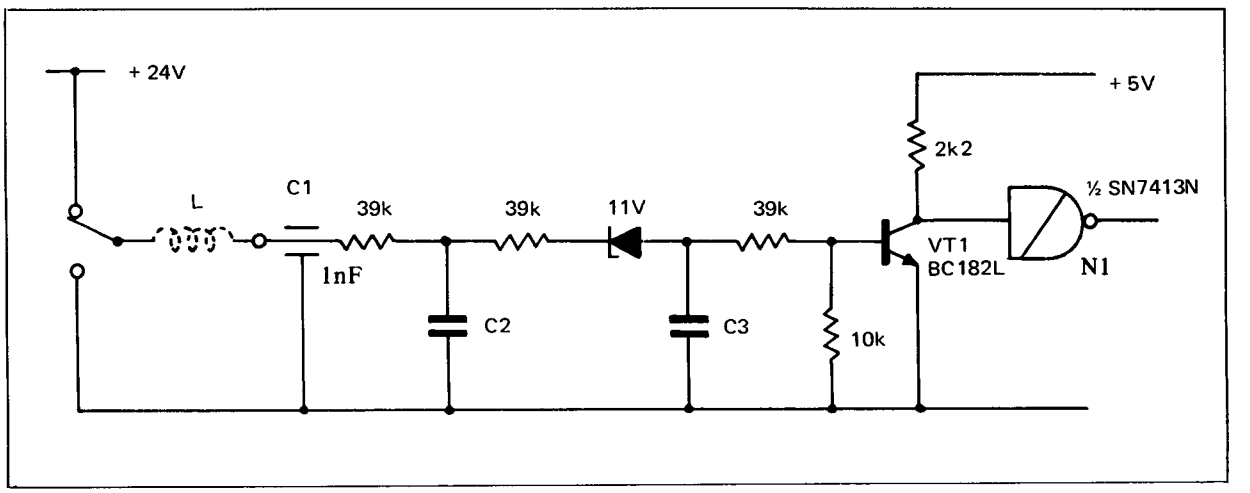


Figure 29.

Optical Interfaces

In many industrial systems it is possible for very large transient common mode voltages to exist between equipments. In cases such as these an isolated coupler such as reed relays, transformers or optical devices must be used in order to transmit date. An alternative is to attenuate the signal and common mode offset until the common mode voltage is sufficiently low to be acceptable. The signal is then detected by a high gain differential comparator. This system does, however, have poor noise rejection unless common mode paths are carefully balanced.

An economical method giving a high degree of isolation (>1kV) and reasonable speed is the optical coupler, as shown in Figure 30.

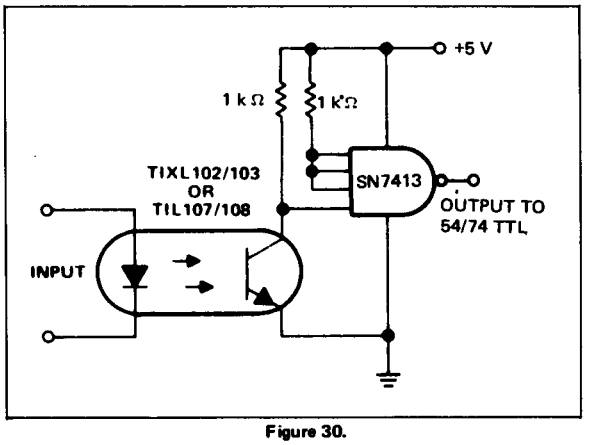


Figure 30.

The optical isolator consists of an infrared emitter and receiver diode electrically isolated from each other, but maintained in the same package. The emitter diode forward current is in the order of 15mA to obtain a receiver current of 2mA (TIL 111). A suitable buffer between the diode output and TTL input must be provided which in the simplest form would be a TTL Schmitt trigger. A maximum bit rate of approximately 60kHz can be obtained with the circuit of Figure 29. If higher bit rates are required then the TIL 111/2 should be followed by a wideband operational amplifier such as the SN7511 operated in the virtual earth mode.

Interface Filters

The previous few circuits have concentrated on the voltage requirements of an interface, although Figures 28 and 29 will be low pass filters.

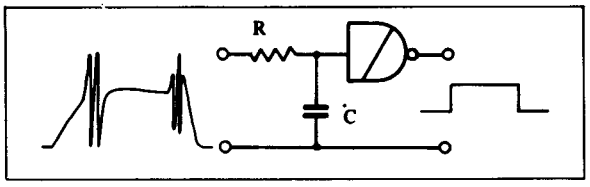


Figure 31.

The filter shown in Figure 30 is all that is needed in the majority of cases, to eliminate noise associated with input signals. To maintain noise immunity at the Schmitt input the maximum value of resistor R should be limited to 250Ω when being driven from standard 74N Series TTL.

This, therefore, determines the value of capacitor C for a given 3dB cut-off frequency, f_0, of the filter, i.e. $C = 1/2\ \Pi\ R.f_0$. The rate of attentuation past the cut-off frequency is 6dB/octave. For larger rates of attentuation and faster response times multipole Chebyshev filters can be used. Since the input to the Schmitt is always positive with respect to ground, capacitor C may be a large value electrolytic.

Low pass filter, Chebyshev

These filters should be used when digital equipment is required to operate under conditions of extreme electrical noise. The Chebyshev filter is characterised by an amplitude frequency response that ripples in the pass band and falls off rapidly past the cut-off frequency f_0. The general form of this type of filter is shown in Figure 31.

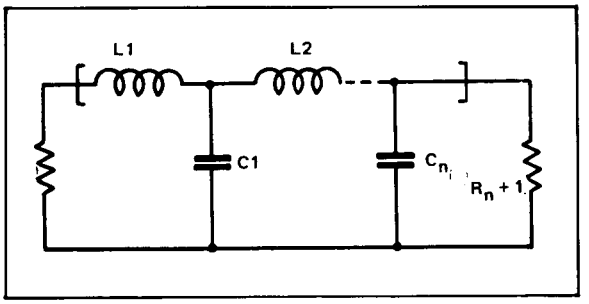


Figure 32.

The amplitude frequency response of such a filter is shown in Figure 32.

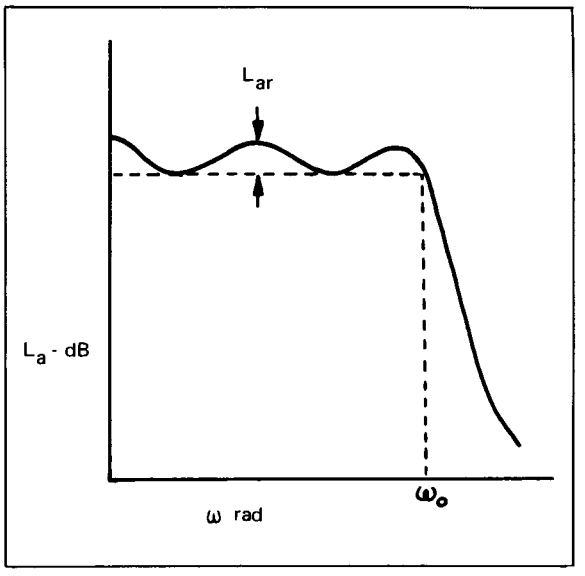


Figure 33.

This circuit form is well suited to mechanical construction since the capacitive elements can be lead throughs. The required D.C. operating conditions for the Schmitt trigger are easily satisfied since the filter has almost zero impedance at D.C.

A compromise has to be made between the number of elements and the rate of attentuation past the cut-off frequency. In practice, a four element filter that has an attenuation of 60dB at $4\omega_o$ is usually satisfactory. The load impedance $R_n + 1$ is determined by the input impedance of the Schmitt trigger, which in turn determines the filter source impedance R_o. For this reason it is more practical to use a different filter design which will match a low source impedance to the input impedance of the Schmitt trigger (4k approx.).

Such a design is shown in Figure 34 and component values are tabulated in Table B for various cut-off frequencies.

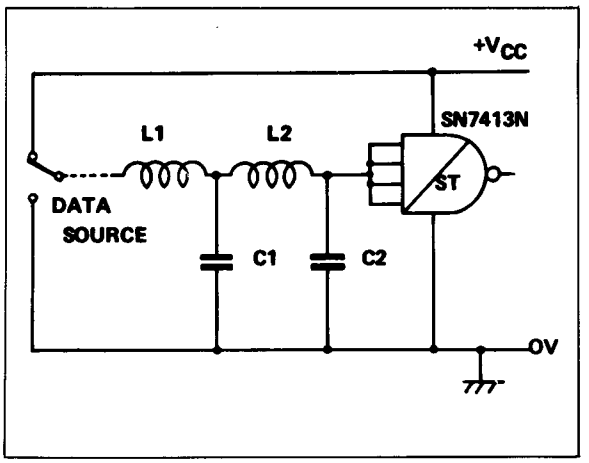


Figure 34.

Element values for 4 element filter with L_{ar} = 1dB and L_a = −60dB at $4\omega_o$.

Table B

f_o(kHz)	L1(mH)	C1(pF)	L2(mH)	C2(pF)
100	9.0	420	8.2	760
200	4.5	220	4.1	380
500	1.8	84	1.6	150
1000	0.9	42	0.8	76

Since the inductive and capacitive components are $\propto 1/f_o$, element values for any cut off frequency f_o may be calculated from the tables given. Additional components may be added to the circuit of Figure 9 to enable it to handle very large voltage surges at the filter input as shown in Figure 35.

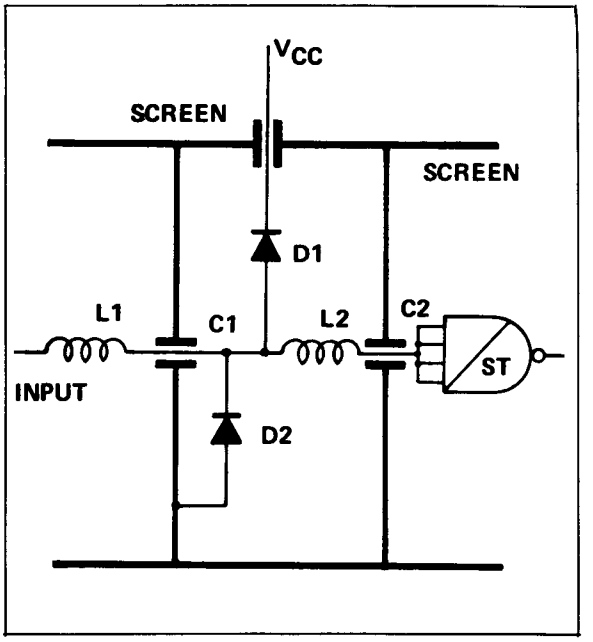


Figure 35.

Diodes D1 and D2 limit the input swing into the Schmitt trigger, they should be situated after inductor L1 so that the rate of rise of voltage across diodes D1 and D2 is limited.

Interfacing to Other Devices

The equipment may require an interface between High Noise Immunity Logic and TTL or between MOS and TTL. Specially for the former there is a HNIL to TTL device (and also one for the opposite direction, TTL to HNIL). MOS to TTL et vice versa is usually simple. Interfacing with the high threshold versions is described fully in report CA170. The low threshold (TTL compatible) types can be interfaced directly, or with perhaps a few resistors.

Memories are another area requiring interfacing. The series 75 sense amplifiers can be used to detect the low output from a core memory or certain MOS memories. They sense the pulse of 20mV or so between two sense lines of the memory plane regardless of its polarity and convert it into a TTL signal. Balanced-line receivers such as the 75107 can be used, as well as for their original purpose, as level detectors or comparators. They have the advantages of high speed, up to about 20MHz, and a full fan-out TTL output. In fact, they make good interfaces between high frequency, low amplitude signals and TTL, such as is required at the input to a frequency counter.

Output Interfacing

A standard TTL output stage can sink 16mA. This is sufficient to operate LEDs and small relays as shown in Figure 36.

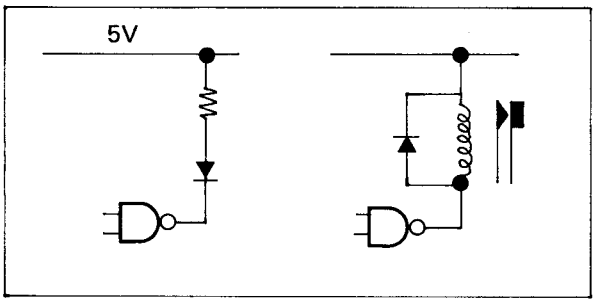


Figure 36.

The LED can be visible or infra-red. It can even be the first half of an Optically Coupled Isolator. Interfacing with CMOS can be achieved as shown in Figure 37.

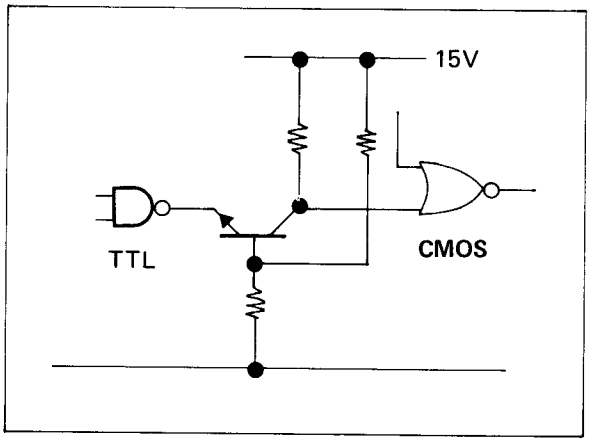


Figure 37.

A gate can drive a SCR for switching on a lamp as in Figure 38.

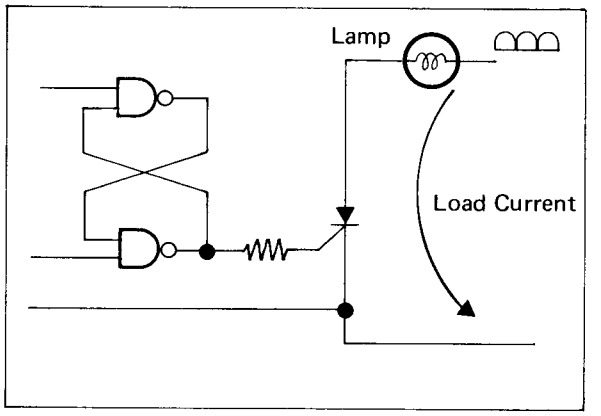


Figure 38.

The SCR solution for driving lamps is useful as it is not affected by the cold current of the lamp which may be 10 or 20 times the nominal operating current of the lamp. Another way of driving a large load without using an SCR is via a transistor. The current into the base which is available from the gate when its output goes high, is at least 70 percent of the minimum specified short circuit current.

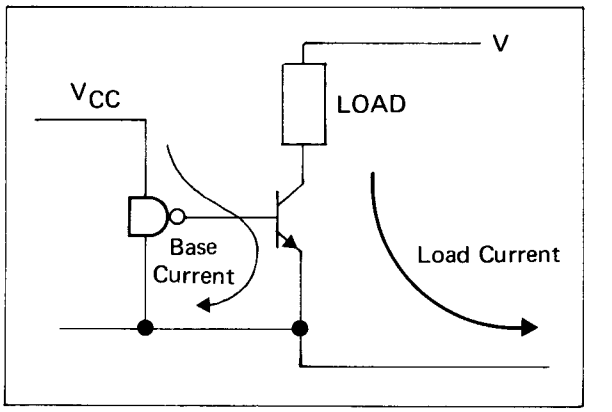


Figure 39.

For more specific outputs there are memory drivers, peripheral drivers and balanced line drivers. There is even a Nixie tube driver. Outputs are an unexpected source of faults.

The output must not inject noise back into the logic, either on the 5V rail or as earth noise. For instance, when laying out the circuits in Figure 38 and 39 it is important to make sure that the load current does not flow along the logic ground line.

Line Driving

When an interconnection is above a certain length depending upon the edge speeds being propagated, it is necessary to consider the interconnection as a transmission line. As the different families within System 74 have different speeds this length will vary from family to family.

Table C

Series	Speed (ns)	length (approx) (cm)	line impedance (Ω)
74	10	50	100
74H	6	50	75-100
74L	33	200	150
74LS	10	50	150
74S	3	25	75
75 (=74)	10	50	100

These lengths are listed in Table C along with a suggested line impedance for using with each series of outputs. Due to the input and output characteristics of TTL very acceptable waveforms can be obtained using System 74.

The following rules have been established for the elimination of transmission-line troubles in TTL systems.

1. Use direct wire interconnections that have no specific ground return for lengths up to about half those in Table C. A ground plane is always desirable.
2. Direct wire interconnections must be routed close to a ground plane if they are longer and should never exceed Table C.

3. When using coaxial or twisted-pair cables, design around approximately 100Ω characteristic impedance for series 74N. Coaxial cable of ≅ 100Ω impedance is recommended. For twisted pair No. 26 or No. 28 S.W.G. wire with thin insulation twisted about 30 turns per foot works well. Higher impedances increase cross talk, and lower impedances are difficult to drive. Use the impedances listed in Table C for other series.
4. Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends.
5. Connect reverse termination at driver output to prevent negative overshoot.
6. Decouple line-driving and line-receiving gates as close to the package V_{CC} and ground pins as practical, with a 0.1 μF capacitor.
7. Gates used as line drivers should be used for that purpose only. Gate inputs connected directly to a line-driving output could receive erroneous inputs due to line reflections, long delay times introduced, or excessive loading on the driving gate.
8. Gates used as line receivers should have all inputs tied together to the line. Other logic inputs to the receiving gate should be avoided, and a single gate should be used as the termination of a line.
9. Any device that derives internal feedback from its outputs should not be used for line driving. Such devices are bistables, shift registers and monostables.
10. Gates that drive back wiring via an edge connector should be mounted near the connector ground in order to provide a low impedance return for line currents.

One of the useful things about System 74 TTL is that it does not need clamp diodes. Clamp diodes are low forward impedance diodes placed under TTL inputs with the object of minimizing "line ringing" or "line reflection" when mismatching occurs between driving and driven gates and the line along which the signal is propagating.

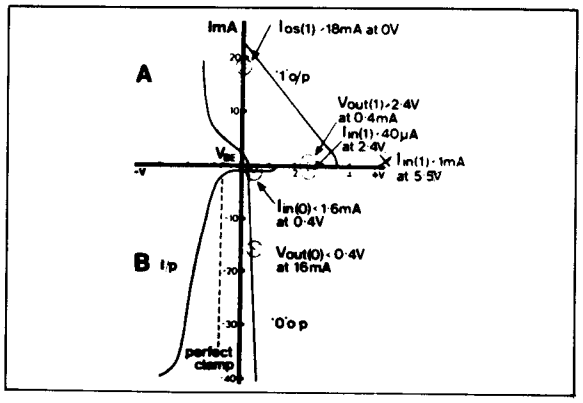


Figure 40.

To perform line ringing calculations one can use a graphical approach. In Figure 40 are the input and output characteristics of a 74N Series gate. The data sheet guaranteed parameters are indicated by the crosses.

Quadrants A and B respectively are the inverse output and inverse input characteristics – areas of operation which are not normally guaranteed, but of vital importance to the study of line ringing phenomena. The B characteristic is usually known as "input clamping". Added is the plot for a perfect clamp at V_{BE} below zero volts.

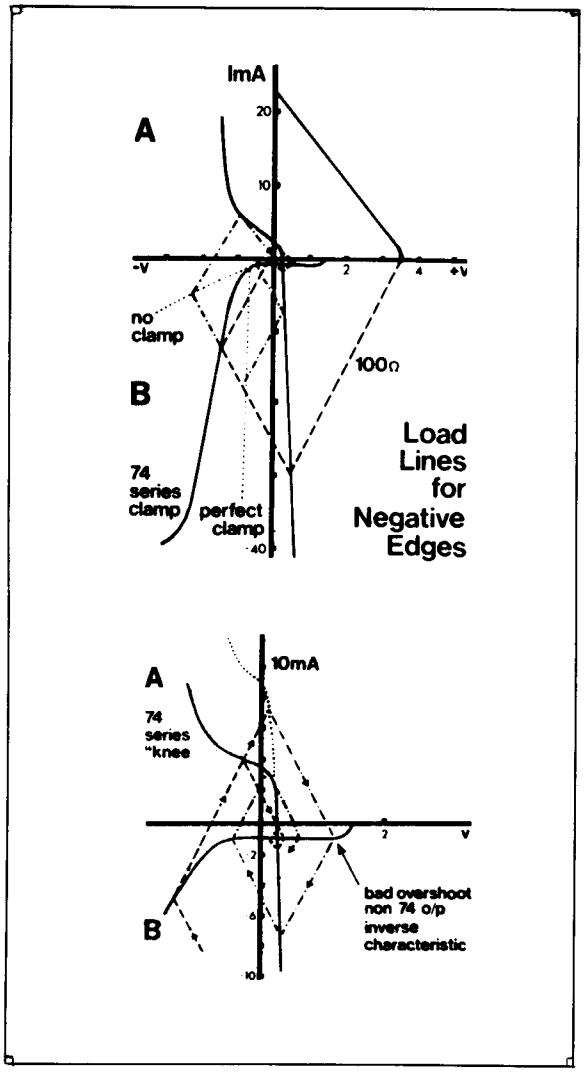


Figure 41.

Load lines are also superimposed on the second diagram with slope equal to line impedance so that line ringing can be calculated for a negative edge of the waveform. These are for a 100 ohm line showing normal 74 Series clamping compared with perfect clamping and no clamping at all. There is virtually no difference in the resulting overshoot for the three cases, and the reason for this is the nature of the characteristic in the A quadrant.

The exact portion of the characteristic which is a design feature of System 74 TTL, is the 'knee' and the point at which it crosses the current axis. If this is pushed up the current axis, bad overshoot results. So we make sure that our process control maintains this knee at about 4mA. In this way we eliminate the need to add extra components to our circuits to modify characteristics in the A quadrant by, for instance, adding clamp diodes.

Quality and Reliability

QUALITY AND RELIABILITY

This subject can be divided into separate areas of discussion. The reliability of components is a function of good design and processing by the manufacturer. The quality of components supplied to the user is a function of measurement and selection. The Quality Assurance personnel are responsible for supplying a defined quality of product and also to perform a continuous monitor of production processing in order to feed back information to manufacturing personnel who can then control processing to maintain quality.

Clearly, this feedback and maintenance of quality during production is important both to the user and producer. No producer can afford to produce such a quality that a significant part is rejected by Q.A. Neither can a Q.A. department tolerate continued rejection of poor quality from production. This situation would mean less product of acceptable quality available to the user at relatively higher cost.

Thus, the Quality Assurance and Reliability department has two distinct functions.

1. To test to a defined quality level by statistical means all product from manufacturing and then either return the product to manufacturing for rescreening or pass them to finished goods inventory.

2. To take random samples of product, straight from production and fully subject these to rigorous 100% electrical, mechanical and environmental testing. The results of this are made available on a quarterly basis in the form of a report. The primary object of this, in addition to providing test results, is to generate a failure rate analysis from which Mean Time Between Failures (MTBF) can be calculated.

These aspects of quality and reliability are discussed below. The third aspect is the feedback obtained from customers. Using this information an in-use failure rate can be estimated from results for major projects in the industry. This is expected to indicate that product quality is better than defined by the Q.A. Department in line with the philosophy of manufacturing product of a higher quality than defined by published quality levels.

QUALITY

In common with most industries supplying components in high volume a statistical method is used to estimate the quality level of product supplied to the customers. It can be shown that to guarantee quality by individual testing would require 300% testing. That is, each component would have to be tested 3 times by different operators using different test equipments. Even at this level of testing some non-perfect components would evade this surveillance. A statistical sampling method is currently used whereby a sample of each production lot submitted to Q.A. is 100% tested and acceptance or rejection of the total lot depends upon the performance of the sample. All lots are 100% tested during the production phase, but this testing is not that used to guarantee the final quality. It is part of the procedure where every production process is monitored and immediate feedback supplied at each process step.

Texas Instruments currently uses an AQL sampling plan. The AQL (Acceptable Quality Level) plan specifies the maximum deviation from perfect quality that is acceptable to the industry. The AQL is considered as that quality of a lot which has a probability of acceptance of 0.95. An inspection level is specified with the AQL which determines the number of samples to be tested. Although the number of samples increases with lot size, the ratio of sample size to lot size decreases.

The defence specification DEF-131-A contains the details of sample size, lot size, and failures permitted for a given AQL and inspection level.

System 74 quality is governed by the following AQL and inspection levels:-

	A.Q.L.	INSPECTION LEVEL
FUNCTIONAL	0.15%	II
D.C. PARAMETERS	1.0%	II
A.C. PARAMETERS	2.5%	I

It is the experience of Texas Instruments that where customers 100% test at goods inward, it is verified that the actual quality supplied is in fact considerably better than the quoted AQL.

Thus, the AQL defines the quality of product shipped to customers. The reliability of that product is not directly related to AQL and is assured by good engineering practice. The method used by Texas Instruments to monitor this is by a continuous surveillance of failure rate and this is discussed under the heading of reliability.

RELIABILITY

Reliability of a device can be defined as the probability that it will deliver without failure a specified performance under specified operating conditions for a required period of time. Thus, reliability can only be achieved through correct design and careful production.

Quality is related to reliability in the following way:-
Reliability is the ability to operate to the electrical specification during the period of utilization.

Quality is conformance to the electrical specification.

Reliability is indicated by the rate of failure with time and the commonly accepted method of stating this is Failure Rate per cent per 1000 hours.

The test conditions used by Texas Instruments for failure rate analysis for System 74 products are as follows:-

TEST CONDITIONS

The operating life tests are carried out in an ambient temperature of 125°C. The devices are connected with V_{CC} = 5V, outputs loaded, and inputs switched at 100KHz.

The environmental test sequence is based on tests laid down in BS9400 and K1007 and is performed in the order indicated below:

1. **Solderability** BS9400 Para. 1.2.6.15.1.

Leads are immersed for 2 secs in molten solder at 230°C after a five second immersion in an inactive flux. To pass the test, leads must have at least a 95% uniform covering of solder under 10x magnification.

2. **Swept Frequency Vibration** BS9400 Para. 1.2.6.8.1.

Devices are vibrated at peak acceleration of 196 m/s^2 at a frequency varying from 150 Hz to 2KHz every ten minutes. This is continued for 2 hours in each of three mutually perpendicular directions.

3. **Moisture Resistance** K1007 Para. 5.3.13. Method C.

The devices are introduced into the climatic chamber and the temperature increased to 65°C over a period of 2–3 hours, with a relative humidity of 90–98%. These conditions are maintained for 3 hours, then the temperature falls to room ambient in 2–4 hours with a R.H. of 80–98%. This procedure is repeated and then the devices are maintained at 90–98% RH and room temperature for 8 hours. This constitutes one cycle, the test consists of 10 continuous cycles.

The extended moisture resistance is carried out on devices having already completed the environmental test sequence. These are returned to the climatic chamber to complete a total of one thousand hours in the chamber.

Tables 1 and 2 summarize the results obtained from life and environmental tests respectively on devices produced since the beginning of 1969. The failure rates obtained from the 125°C operating life tests have been converted to the equivalent failure rate at 55°C, using a procedure described in the "1966 Proceedings of the Annual Symposium on Reliability".

Two distinct classes of failure are reported herein, functional and parametric. A functional failure is a device which fails to perform its published truth table and hence would cause an equipment malfunction. A parametric failure is a device which while continuing to perform its published logic function, fails to meet its data sheet parameter limits. A parametric failure will often not cause an equipment malfunction. The two are distinguished in the tables by the letters P and F.

TABLE 1

FAILURE RATE INFORMATION WITH REFERENCE TO MANUFACTURING PERIOD. SN74N SERIES OPERATING LIFE TEST

Year of Manufacture		1969	1970	1971	1972	TOTAL
Sample Size		1155	720	818	540	3233
Test K Hrs @ 125°C		2000	2867	3162.2	940	8969.2
Equivalent Test K Hours @ 55°C		9600	13762	15178	4512	43052
Failures P/F		2/2	4/3	0/5	0/0	6/10
Failure Rate 90% Conf. %/K Hr.	Overall P + F	0.083	0.082	0.06	0.05	0.051
	Funct. only	0.054	0.048	0.06	0.05	0.035

P—Parametric failures F—Functional failures Parametric figures do not include functional failures.

TABLE 2

ENVIRONMENTAL TEST SEQUENCE

Year of Manufacture	1969	1970	1971	1972	TOTAL
Sample Size	650	400	320	100	1470
Failures P/F	0/0	0/2	0/0	0/0	0/2
Solderability Failures	0	0	0	1	1
No. on extended moisture	350	200	190	60	800
Failures P/F	0/0	0/0	0/1	0/0	0/1

FAILURE RATE CALCULATIONS

The upper 90% confidence limit is determined in the following way:

$$n = (f + 1)\left\{1 - \left(\frac{1}{9(f+1)}\right) + d\sqrt{\frac{1}{9(f+1)}}\right)^3$$

where f = No. of failures observed
d = confidence factor

$$\text{then } \lambda = \frac{100\,n}{\text{No. of device K Hours on test}} \text{ \%/K Hr.}$$

The failure rate calculated in this way is always higher than the observed failure rate, but in 90% of instances the failure rate of the product will be below this value.

TEMPERATURE ACCELERATION FACTORS

For some years it has been agreed that temperature is a prime accelerating mechanism for failure rates of semiconductor devices. It has been found by experiment that if failure rate is plotted on a log scale against the inverse of wafer temperature in absolute degrees, a straight line is obtained.

A number of laboratories have verified this and produced quantitative results. The figures for this report are taken from the "1966 Annual Symposium on Reliability"; from the data presented there the following acceleration factors have been calculated:

$$(\lambda \text{ @ } 25°C) = \frac{(\lambda \text{ @ } 55°C)}{2.5} = \frac{(\lambda \text{ @ } 70°C)}{3.5} = \frac{(\lambda \text{ @ } 125°C)}{12}$$

$$(\lambda \text{ @ } 55°C) = \frac{(\lambda \text{ @ } 70°C)}{1.4} = \frac{(\lambda \text{ @ } 125°C)}{4.8} = \frac{(\lambda \text{ @ } 150°C)}{6.6}$$

SUMMARY

Since January 1969, the QRA Laboratory at Texas Instruments Ltd., Bedford have tested over three thousand plastic integrated circuits on max. rated life test at 125°C. All devices completed 1000 hours and about a half were continued to 5000 hours, the equivalent of nearly three years' continuous operation at 55°C. The equivalent of more than forty three million device hours at 55°C have been accumulated, and sixteen failures have occurred, only ten of which were functional failures.

During the same period, almost fifteen hundred devices have been subjected to the environmental test sequence. Only four failures have occurred.

This report predicts, with 90% confidence, that the failure rate of plastic encapsulated TTL integrated circuits operating in an ambient temperature of 55°C will be better than 0.035%/KHr.

The final most recent figure for failure rate shown can be used to estimate MTBF (Mean Time between Failures).

$$\text{MTBF} = \frac{1}{\text{FAILURE RATE}}$$

Related to a single device this states how reliable a component is during its useful life.

In a system of series components (i.e. if one fails, the system fails) the MTBF of the system is:-

EXAMPLE a) Single Component
Failure Rate = 0.35%/KHrs.

$$\text{MTBF} = \frac{1000 \times 100}{0.035}$$

$$\simeq 3 \times 10^6 \text{ Hrs.}$$

b) System—1000 Series Components

$$\text{System MTBF} = \frac{3 \times 10^6 \text{ Hrs.}}{1000}$$

$$\simeq 3000 \text{ Hrs.}$$

The test conditions used to establish the published failure rate are clearly very rigorous and do not apply to the majority of systems actually in operation. Thus, returned information from major users allows a different look at failure rate. That is, in-use failure rate.

The difference between published failure and in-use failure rate can be attributed to the following typical factors.

TI "WORST CASE" TESTING PROCEDURES

*Environmental stressing to BS9400.
*Storage Life performed at maximum data sheet limits. Operating Life performed in Accelerated burn-in conditions.
*Humidity environment twice world's worst condition.
*Incompasses only limited temperature devices.
*No special electrical/environmental screening or preconditioning.
*Comprehends both catastrophic and degradation failures.
*Utilizes conservative temperature related derating factors.

ACTUAL FIELD USE CONDITIONS

*Manufacturing and applications less than BS9400 enviroments.
*Storage and operation seldom at maximum rated conditions.
*Operation in controlled enviroments.
*Commercial/Computer utilizes limited temperature devices.
*Varied screening and preconditioning depending on applications.
*"Failure to Function" used as failure defect criteria.
*No derating factors—Normal system applications.

The value of in-use failure rate for Texas Instrument plastic dual-in-line is currently estimated at 0.009%/KHrs.

In the system previously described the System MTBF would be as follows:-

EXAMPLE

a) Single component

Failure Rate = 0.009%/KHrs.

$$\text{MTBF} = \frac{1000 \times 100}{0.009}$$

$$= 10^7 \text{ Hrs}$$

b) System 1000 series components

$$\text{SYSTEM MTBF} = \frac{10^7}{1000}$$

$$\simeq 10{,}000 \text{ Hrs}$$

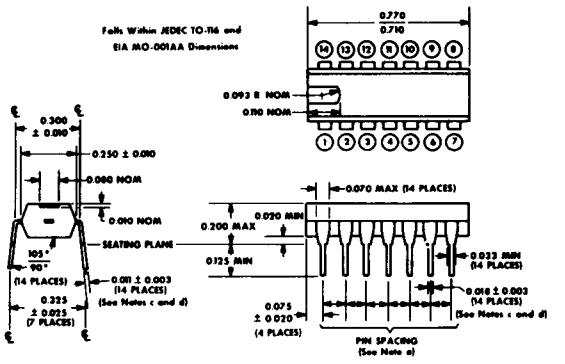
Therefore, as a result of the Texas Instruments philosophy of "worst case" reliability testing, and with reasonable considerations, the customer may enjoy device reliability levels as great as one order of magnitude in excess of those published by Texas Instruments.

Ordering Instructions
Mechanical Data

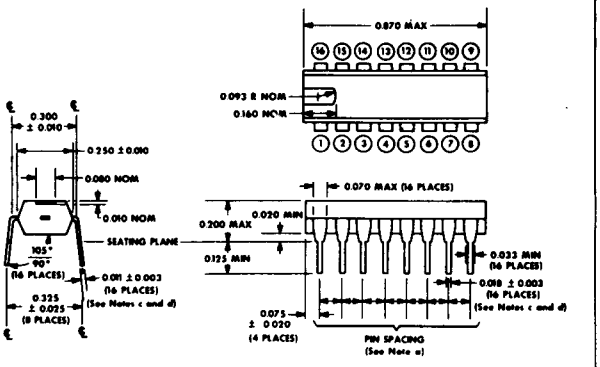
N PLASTIC DUAL-IN-LINE PACKAGES (INCH DIMENSIONS)

These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300 inch (or 0.600 inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

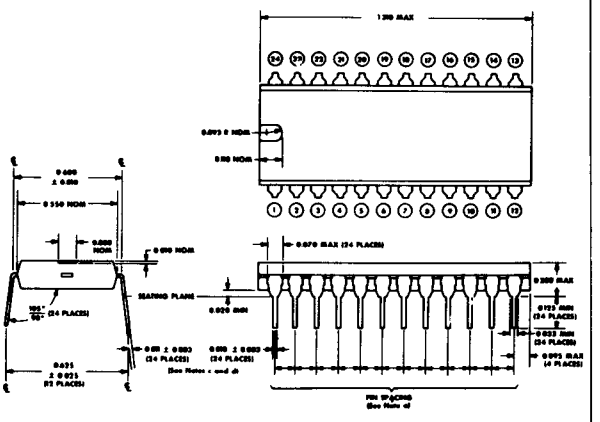
14-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



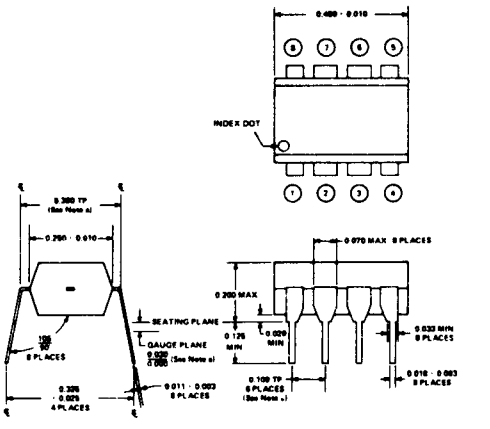
16-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



24-PIN N PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



8-PIN P PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES a. Each pin is within 0.005 radius of true position (TP) at the guage plane with maximum material condition and unit installed.

b. All dimensions are in inches unless otherwise noted.

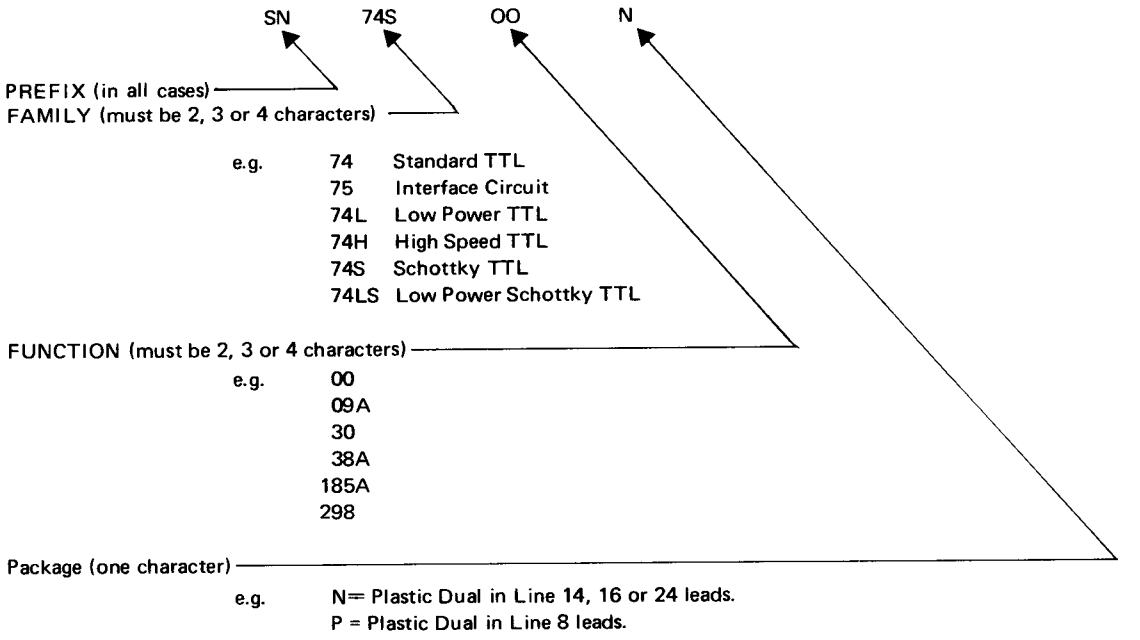
P PLASTIC DUAL-IN-LINE PACKAGE

This dual-in-line package consists of a circuit mounted on a 8 lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300 inch centers. Once the leads are compressed to 0.300 inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

ORDERING INSTRUCTIONS AND MECHANICAL DATA

The complete number of any device type in System 74 must be quoted when ordering. The number quoted consists of four parts.

Example



ABBREVIATIONS USED IN SELECTION GUIDE

O/P	Output	PROM	Programmable Read Only Memory
O/C	Open Collector	SSI	Small Scale Integration
A/O	And-Or	MSI	Medium Scale Integration
AOI	And-Or-Invert	PIPO	Parallel In Parallel Out
ROM	Read Only Memory	PISO	Parallel in Serial out
RAM	Random Access Memory	SIPO	Serial in Parallel out
		SISO	Serial in Serial out

Circuit Selection Guide

Circuit Selection Guide: TTL

TYPE	FUNCTION	74N	74HN	74LN	74LSN	74SN	Gates	Flip-Flops	Latches	Counters	Shift Registers	Decoders	Data Selectors	Arithmetic Functions	Memories	Others	No. of Pins
00	Quad 2 Input Nand	■	■	■	■	■	■										14
01	Quad 2 Input Nand O/C	■	■		■		■										14
01A	Quad 2 Input Nand 15V O/P	■					■										14
02	Quad 2 Input Nor	■		■	■	■	■										14
03	Quad 2 Input Nand O/C	■		■	■	■	■										14
03A	Quad 2 Input Nand 15V O/P	■					■										14
04	Hex Inverter	■	■	■	■	■	■										14
05	Hex Inverter O/C	■	■		■	■	■										14
05A	Hex Inverter 15V O/P	■					■										14
06	Hex Inverter / Buffer 30V O/P	■					■										14
07	Hex Buffer 30V O/P	■					■										14
08	Quad 2 input And	■			■		■										14
09	Quad 2 Input And O/C	■			■		■										14
09A	Quad 2 Input And 15V O/P	■					■										14
10	Triple 3 input Nand	■	■	■	■	■	■										14
11	Triple 3 input And		■		■	■	■										14
12	Triple 3 input Nand O/C	■					■										14
12A	Triple 3 Input Nand 15V O/P	■					■										14
13	Dual 4 Input Nand Schmitt	■					■										14
14	Hex Inverter Schmitt	■					■										14
15	Triple 3 Input And		■		■	■	■										14
16	Hex Inverter/Buffer 15V O/P	■					■										14
17	Hex Buffer 15V O/P	■					■										14
20	Dual 4 Input Nand	■	■	■	■	■	■										14
21	Dual 4 Input And		■		■	■	■										14
22	Dual 4 Input Nand O/C	■	■		■	■	■										14
22A	Dual 4 Input Nand 15V O/P	■					■										14
23	Dual 4 Input Nor-Strobe	■					■										16
25	Dual 4 Input Nor-Strobe	■					■										14
27	Triple 3-Input Nor	■			■		■										14
28	Quad 2-Input Nor Buffer	■			■		■										14
30	8-Input Nand	■	■	■	■	■	■										14
32	Quad 2-Input Or	■			■		■										14
33	Quad 2-Input Nor Buffer O/C	■			■		■										14
33A	Quad 2-Input Nor Buffer 15V	■					■										14
37	Quad 2-Input Nand Buffer	■			■		■										14
38	Quad 2-Input Nand Buffer O/C	■			■		■										14
38A	Quad 2-Input Nand Buffer 15V	■					■										14
40	Dual 4-Input Nand Buffer	■	■		■	■	■										14
42	BCD - Decimal Decoder	■		*								■					16
43	Excess 3-Decimal Decoder	■		*								■					16
44	Excess 3 Gray-Decimal Decoder	■		*								■					16
45	BCD - Decimal Decoder 30V O/P	■										■					16
46A	BCD - Seven Segment Decoder 30V O/P	■		*								■					16
47A	BCD - Seven Segment Decoder 15V O/P	■		*								■					16
48	BCD - Seven Segment Decoder	■										■					16
50	Dual 2-wide 2-Input AOI	■	■				■										14
51	Dual 2-wide 2-Input AOI	■	■	■	■	■	■										14
52	Expandable 2-2-2-3 Input AO		■				■										14
53	4-wide 2-Input AOI	■	■				■										14
54	4-wide 2-Input AOI	■	■	■	■		■										14
55	Expandable 2-wide 4-Input AOI		■	■	■		■										14
60	Dual 4-Input Expander	■	■				■										14
61	Triple 3-Input Expander		■				■										14
62	3-2-2-3-Input AO Expander		■				■										14
64	4-2-3-2 Input AOI					■	■										14

Circuit Selection Guide: TTL

TYPE	FUNCTION	74N	74HN	74LN	74LSN	74SN	Gates	Flip-Flops	Latches	Counters	Shift Registers	Decoders	Data Selectors	Arithmetic Functions	Memories	Others	No. of Pins
65	4 - 2 - 3 - 2 - Input AOI					■	■										14
70	J - K Flip-Flop (And Inputs)	■						■									14
71	Flip-Flop		■	■				■									14
72	J–K Flip-Flop (And Inputs)	■	■	■				■									14
73	Dual J–K Flip-Flop	■	■	■	■			■									14
74	Dual D-Type Flip-Flop	■	■	■	■	■		■									14
75	Quad Latch	■		*					■								16
76	Dual J–K Flip-Flop	■	■		■			■									16
78	Dual J–K Flip-Flop		■	■	■			■									14
80	Gated Full Adder	■												■			14
81A	16-Bit Random Access Memory	■													■		14
82	2-Bit Binary Full Adder	■												■			14
83A	4-Bit Binary Full Adder	■			■									■			16
84A	16-Bit Random Access Memory	■													■		16
85	4-Bit Comparator	■		■		■								■			16
86	Quad Exclusive Or	■		■	■	■										■	14
87	4-Bit True/Complement Zero/One Element		■													■	14
88	256 Bit Read Only Memory	■													■		16
89	64 Bit Random Access Memory	■													■		16
90A	Decade Counter	■		■						■							14
91A	8 Bit Shift Register SISO	■		■							■						14
92A	Divide by 12 Counter	■								■							14
93A	4 Bit Binary Counter	■		■						■							14
94	4 Bit Shift Register PISO	■									■						16
95A	4 Bit Shift Register PIPO	■		■	■						■						14
96	5 Bit Shift Register PIPO	■		*							■						16
97	6 Bit Binary Rate Multiplier	■														■	16
98	4 Bit Data Selectors/Storage Registers			■									■				16
99	4 Bit Right-Shift Left-Shift Register			■							■						16
100	Dual Quad Latch	■							■								24
101	J–K Flip-Flop		■					■									14
102	J–K Flip-Flop (And Inputs)		■					■									14
103	Dual J–K Flip-Flop		■					■									14
104	Gated J–K Flip-Flop	■						■									14
105	Gated J–K Flip-Flop	■						■									14
106	Dual J–K Flip-Flop		■					■									16
107	Dual J–K Flip-Flop	■						■									14
108	Dual J–K Flip Flop		■					■									14
109	Dual J–K Flip-Flop	■			■			■									14
110	J–K Flip-Flop Data Lockout	■						■									14
111	Dual J–K Flip-Flop Data Lockout	■						■									16
112	Dual J–K Flip-Flop				■	■		■									16
113	Dual J–K Flip-Flop				■	■		■									14
114	Dual J–K Flip-Flop				■	■		■									14
116	Dual Quad Latch	■							■								24
118	Hex S–R Latch	■							■								16
119	Hex S–R Latch	■							■								24
120	Dual Pulse Synchroniser	■														■	16
121	Monostable Multivibrator	■		*				■									14
122	Monostable Multivibrator	■		*				■									14
123	Dual Monostable Multivibrator	■		*				■									16
125	Quad 3 State Buffer	■					■										14
126	Quad 3 State Buffer	■					■										14
128	Quad 2-Input Nor Line Driver	■					■										14
132	Quad 2-Input Nand Schmitt	■				■	■										14
133	13 Input Nand					■	■										16

Circuit Selection Guide: TTL

TYPE	FUNCTION	74N	74HN	74LN	74LSN	74SN	Gates	Flip-Flops	Latches	Counters	Shift Registers	Decoders	Data Selectors	Arithmetic Functions	Memories	Others	No. of Pins
134	12-Inputs 3 State Nand					■	■										16
135	Quad Exclusive Or/Nor					■										■	14
136	Quad Exclusive Or O/C	■			■											■	14
138	3 Line to 8 Line Decoder/Demultiplexer				■	■						■					16
139	Dual 2 Line to 4 Line Decoder/Demultiplexer				■	■						■					16
140	Dual 4 Input Nand Line Driver					■	■										14
141	BCD - Decimal Decoder/Driver	■										■					16
142	Counter-Latch-Decimal Decoder/Driver	■														■	16
143	Counter-Latch - 7 Segment Decoder/Driver	■														■	24
144	Counter-Latch - 7 Segment Decoder/Driver	■														■	24
145	BCD - Decimal Decoder/Driver 15V O/P	■										■					16
147	10 to 4 Line Priority Encoder	■														■	16
148	8 to 3 Line Priority Encoder	■														■	16
150	16-Bit Data Selector	■											■				24
151	8-Bit Data Selector	■			■	■							■				16
153	Dual 4 to 1 Line Selector	■		*	■	■							■				16
154	4 - 16 Line Decoder	■		*								■					24
155	Dual 2 to 4 Line Decoder	■			■							■					16
156	Dual 2 to 4 Line Decoder O/C	■										■					16
157	Quad 2 to 1 Line Selector	■		*		■							■				16
158	Quad 2 Line to 1 Line Selector Inverting					■							■				16
159	4 to 16 Line Decoder	■										■					24
160	Synchronous Decade Counter	■								■							16
161	Synchronous Binary Counter	■								■							16
162	Synchronous Decade Counter	■								■							16
163	Synchronous Binary Counter	■								■							16
164	8-Bit Shift Register SIPO	■		*							■						14
165	8-Bit Shift Register PISO	■									■						16
166	8 Bit Shift Register PISO	■									■						16
167	4 Bit Decade Rate Multiplier	■														■	16
170	4 by 4 Register File	■													■		16
172	16 Bit Quadriport Register File	■													■		24
173	Quad 3 State Latch	■							■								16
174	Hex D-Type Flip-Flop	■			■	■		■									16
175	Quad D-Type Flip-Flop	■			■	■		■									16
176	Decade Counter	■								■							14
177	Binary Counter	■								■							14
178	4 Bit Shift Register PIPO	■									■						14
179	4 Bit Shift Register PIPO	■									■						16
180	8 Bit Parity Generator	■												■			14
181	4 Bit Arithmetic Logic Unit	■			■	■								■			24
182	Carry-Look-Ahead Unit	■				■								■			16
183	Dual Carry-Save Full Adder		■											■			14
184	BCD - to - Binary Converter	■														■	16
185A	Binary to BCD Converter	■														■	16
186	512 Bit PROM Fusible	■													■		24
187	1024 Bit Read-only-Memory	■													■		16
188	256 BIT PROM Fusible	■													■		16
190	Reversible Decade Counter	■			■					■							16
191	Reversible Binary Counter	■			■					■							16
192	Reversible Decade Counter	■		■	■					■							16
193	Reversible Binary Counter	■		■	■					■							16
194	4-Bit Shift Register PIPO	■			■	■					■						16
195	4-Bit Shift Register PIPO	■			■	■					■						16
196	Decade Counter	■			■					■							14
197	Binary Counter	■			■					■							14

Circuit Selection Guide: TTL

TYPE	FUNCTION	74N	74HN	74LN	74LSN	74SN	Gates	Flip-Flops	Latches	Counters	Shift Registers	Decoders	Data Selectors	Arithmetic Functions	Memories	Others	No. of Pins
198	8 Bit Shift Register PIPO	■									■						24
199	8 Bit Shift Register PIPO	■									■						24
200	256 Bit Random Access Memory	■				■									■		16
206	256 Bit Read/Write Memory O/C					■									■		16
251	8 Input Selector 3 State	■			■	■							■				16
253	Dual 4 Line to 1 Line Selector 3 State				■								■				16
257	Quad 2 Line to 1 Line Selector 3 state Non-Inv.					■							■				16
258	Quad 2 Line to 1 Line Selector 3 State Inv.					■							■	■			16
260	Dual 5 Input Nor Gate					■	■										14
266	Quad 2 Input Exclusive Nor O/C				■		■										14
278	4 Bit Priority Register	■												■			16
279	Quad R–S Latch	■							■								16
280	9 Bit Parity Generator/Checker					■								■			14
283	4 Bit Full Adder	■												■			16
284	4 x 4 Multiplier	■												■			16
285	4 x 4 Multiplier	■												■			16
290	Decade Counter	■								■							14
293	4 Bit Binary Counter	■								■							14
295	4 Bit Right Shift Left Shift 3 State Register				■						■						14
298	Quad 2 Input Multiplexer with Storage	■											■				16

Interface

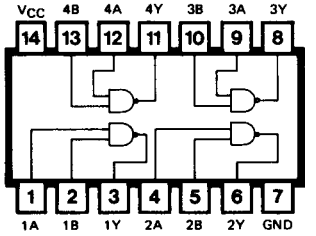
TYPE	FUNCTION	Sense Amplifiers	Line Receivers	Line Drivers	Memory Driver	Peripheral Drivers	Others	No. of Pins
7520	Dual Channel Sense Amp with Complementary Outputs	■						16
7521	Dual Channel Sense Amp with Complementary Outputs	■						16
7522	Dual Channel Sense Amplifier	■						16
7523	Dual Channel Sense Amplifier	■						16
7524	Dual Sense Amplifier	■						16
7525	Dual Sense Amplifier	■						16
7526	Dual Channel Sense Amp with Output Data Registers	■						16
7527	Dual Channel Sense Amp with Output Data Registers	■						16
7528	Dual Sense Amplifier with Pre-amp Test Points	■						16
7529	Dual Sense Amplifier with Pre-amp Test Points	■						16
75107A	Dual Line Receivers		■					14
75108A	Dual Line Receivers		■					14
75109	Dual Line Drivers			■				14
75110	Dual Line Drivers			■				14
75150	Dual Line Drivers			■				14, 8
75154	Quadruple Line Receivers		■					16
75234	Dual Sense Amplifier	■						16
75235	Dual Sense Amplifier	■						16
75238	Dual Sense Amplifier with Pre-Amp Test Points	■						16
75239	Dual Sense Amplifier with Pre-Amp Test Points	■						16
75324	Memory Driver with Decode Inputs				■			14
75325	Memory Driver				■			16
75450A	Dual Peripheral Positive And Driver					■		14
75451A	Dual Peripheral Positive And Driver					■		8
75452	Dual Peripheral Positive Nand Driver					■		8
75453	Dual Peripheral Positive Or Driver					■		8
75454	Dual Peripheral Positive Nor Driver					■		8

Pin Configuration Guide

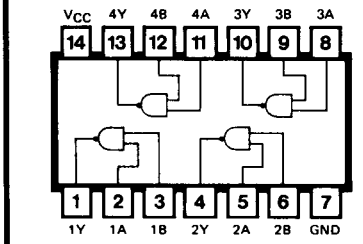
Pin Configuration Guide

Where only one Pin Configuration diagram is shown for a particular function, all versions are the same. Where alternative versions of the same function have different Pin Configurations these are shown. Where the Input Loading for a particular function is other than unity, the Loading Factor is shown in bold figures next to the relevant Input.

00



01



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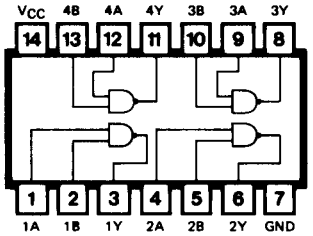

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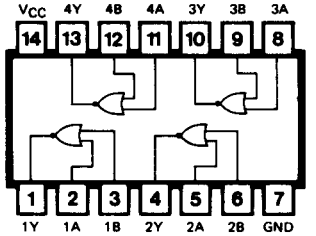

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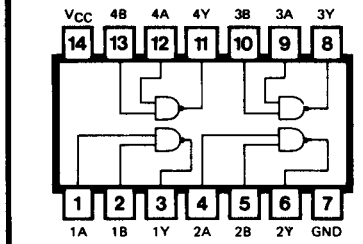

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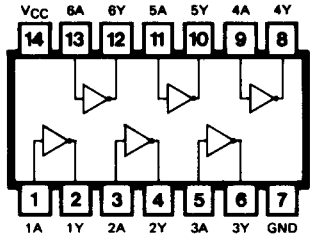

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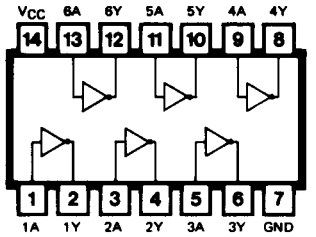

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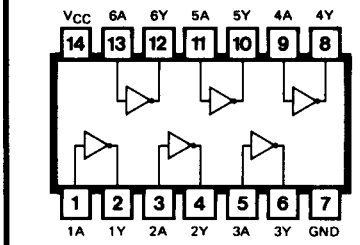

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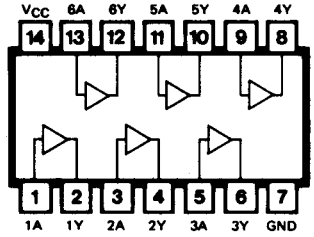

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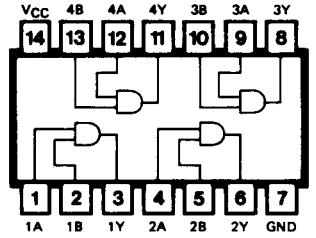
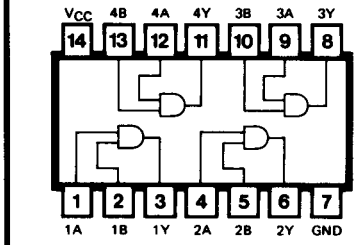


09



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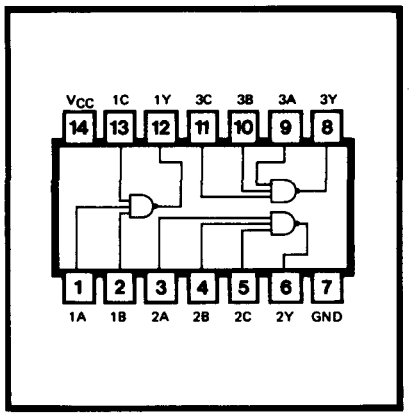

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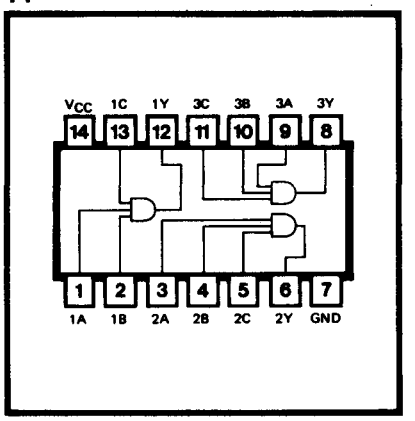

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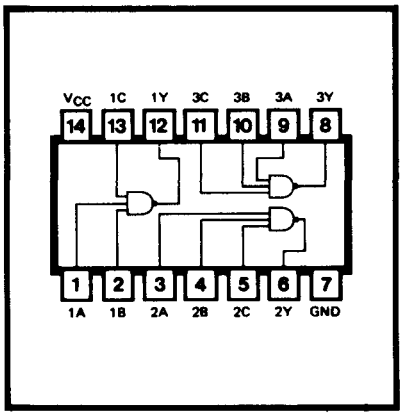

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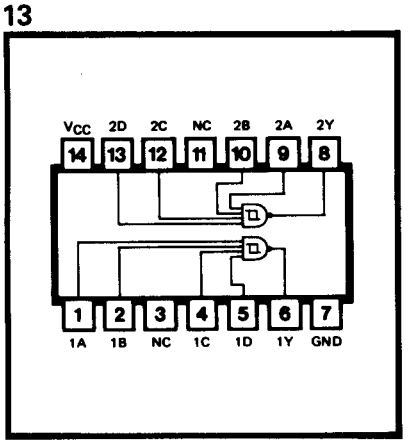

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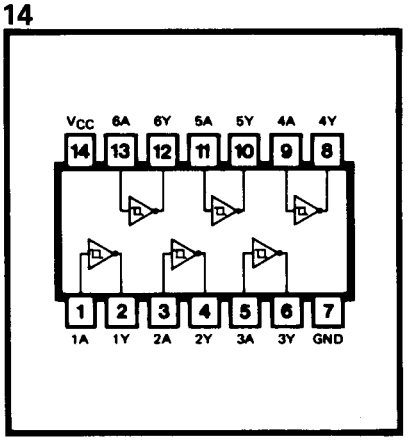

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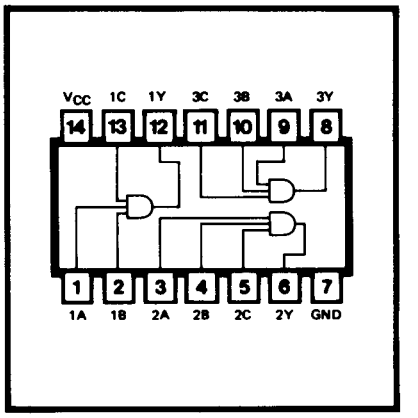

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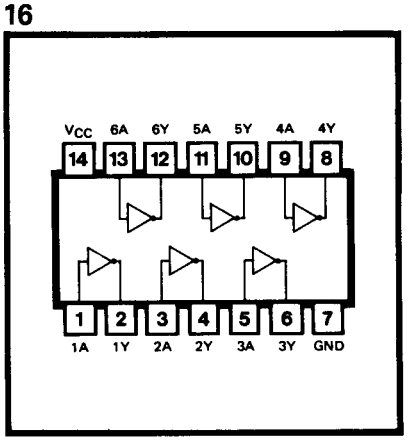

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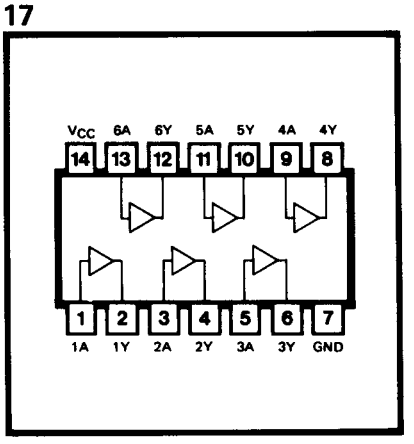

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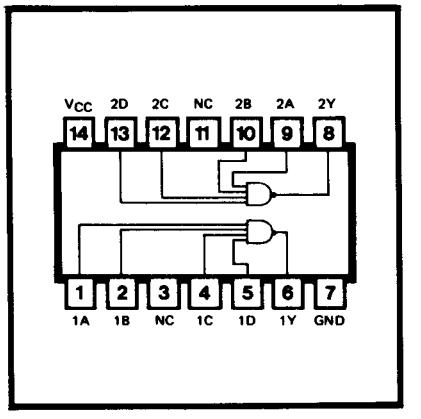

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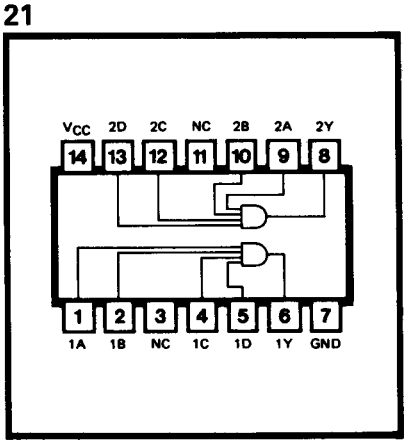

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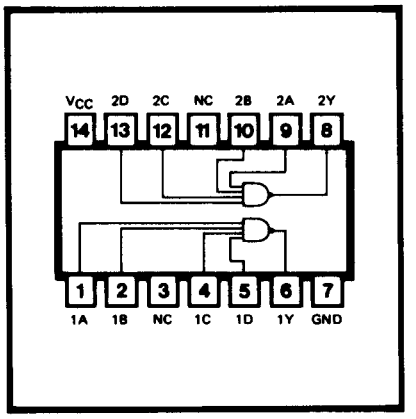

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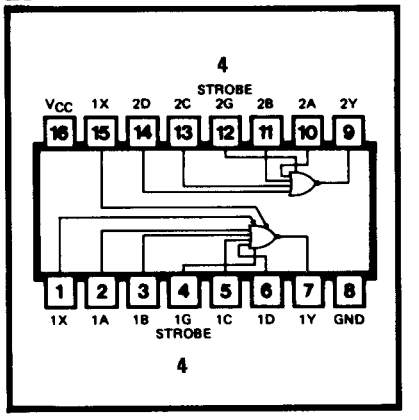

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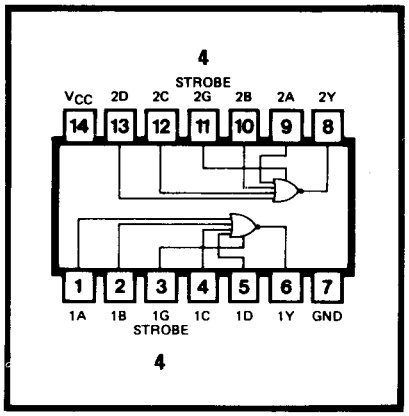

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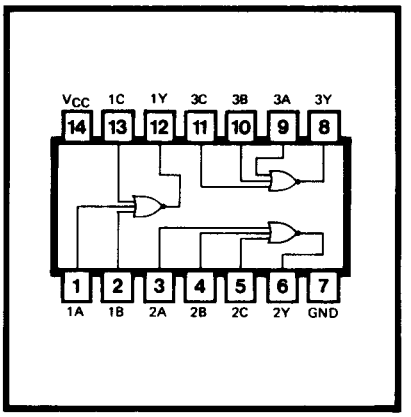

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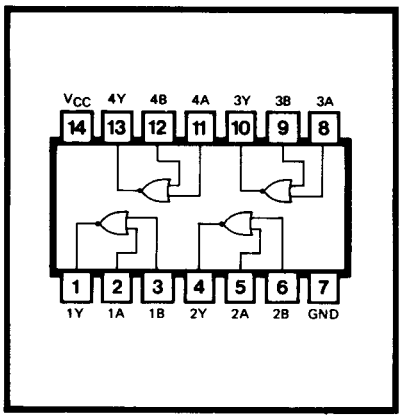

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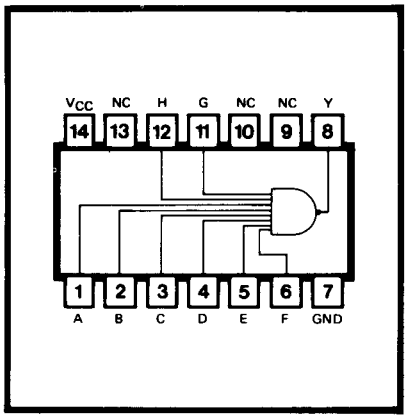

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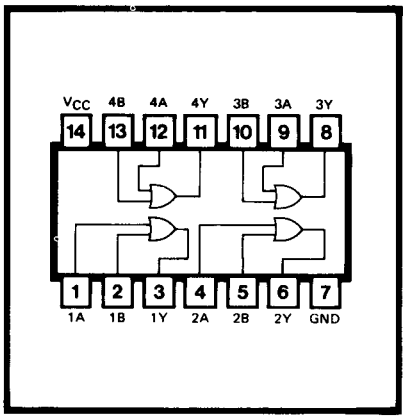

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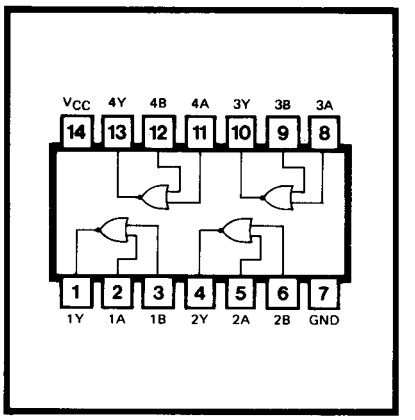

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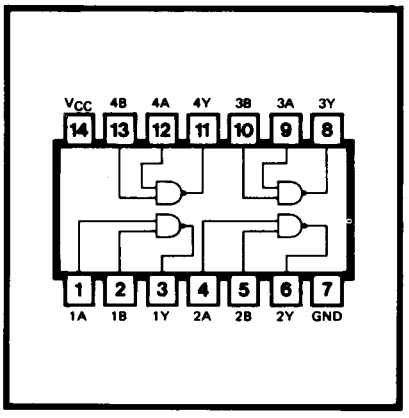

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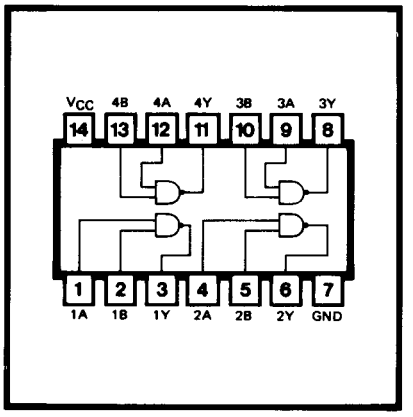

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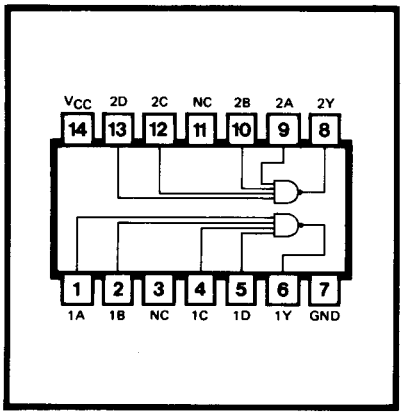

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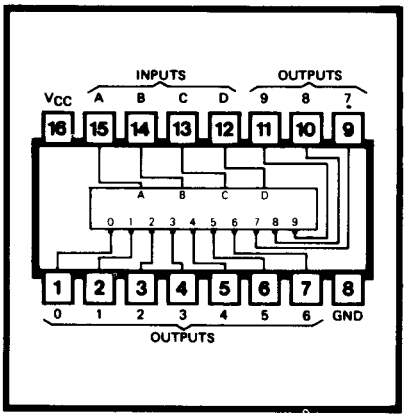

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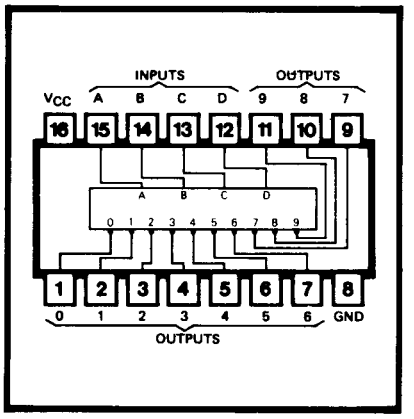

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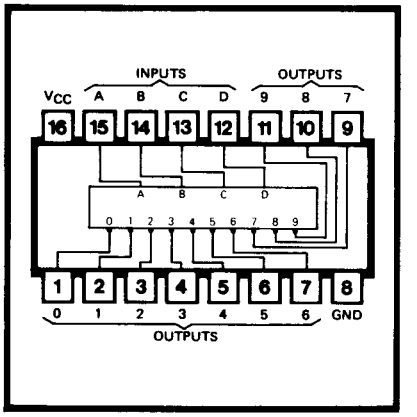

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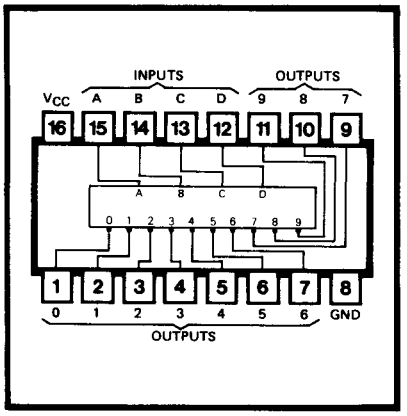

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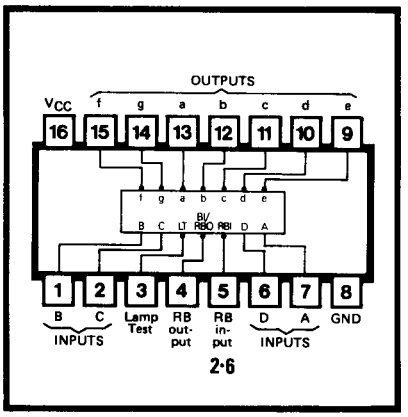

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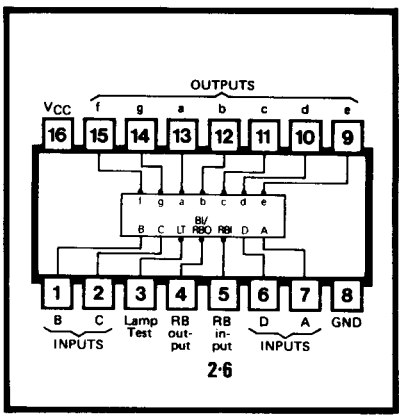

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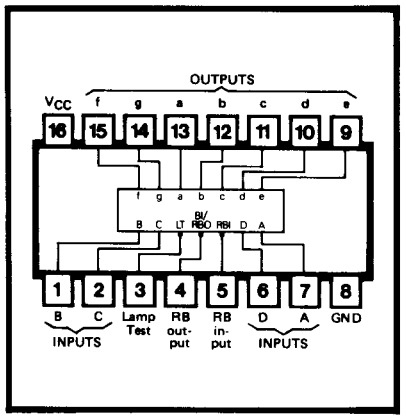

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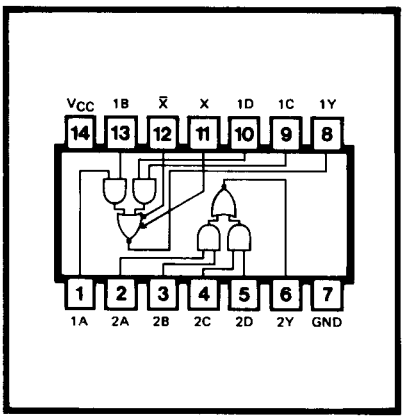

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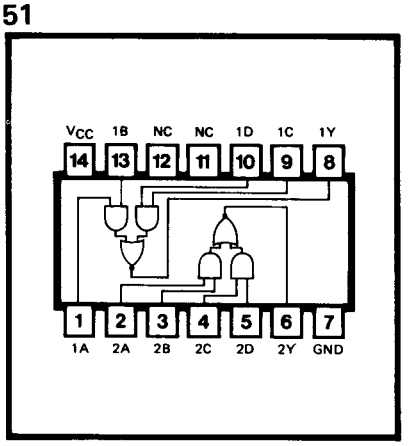

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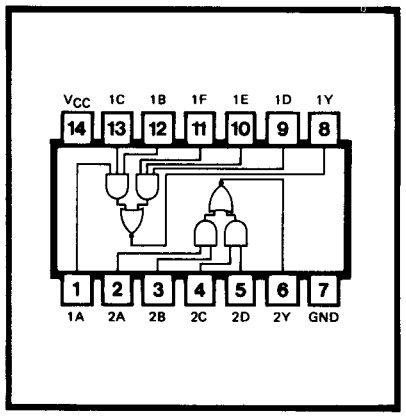

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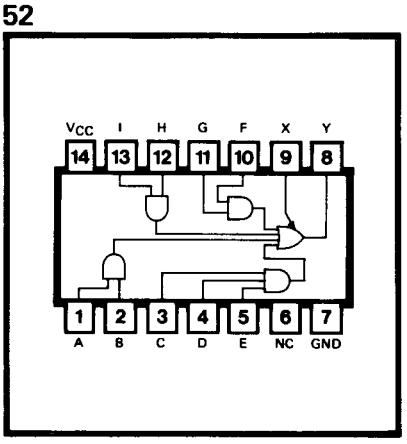

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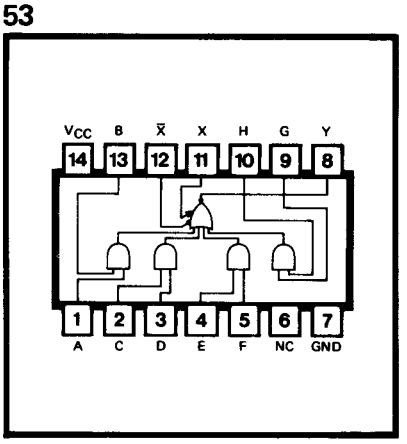

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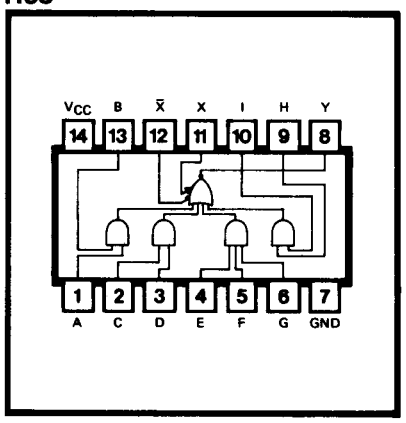

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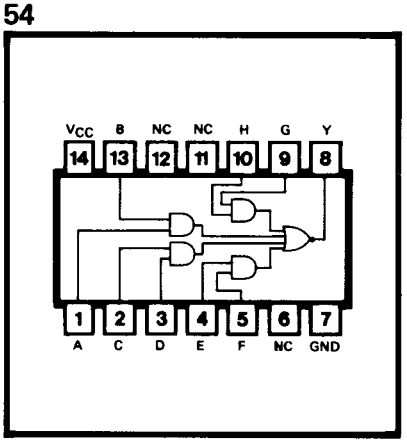

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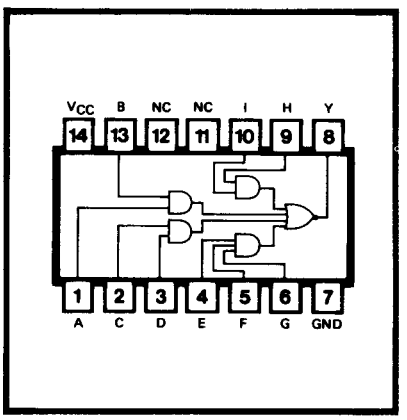

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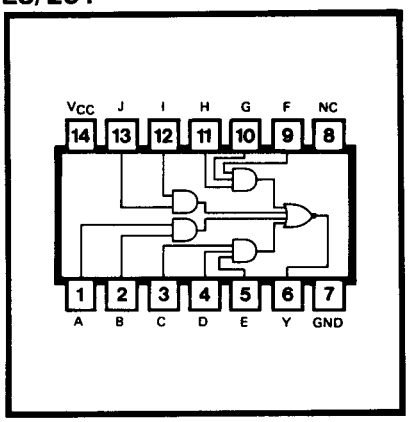

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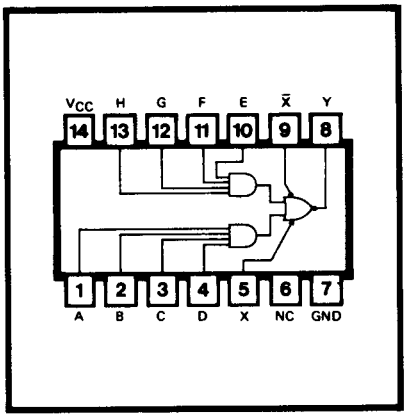

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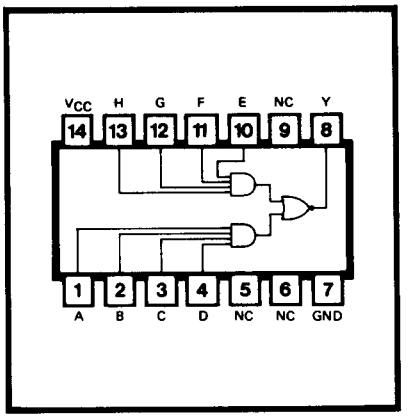

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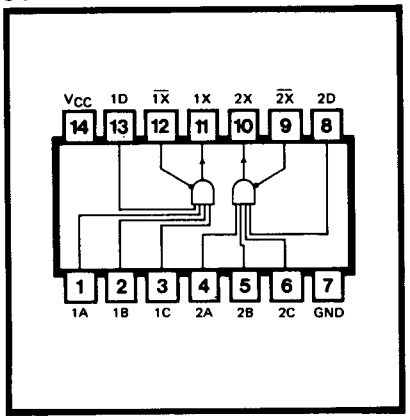

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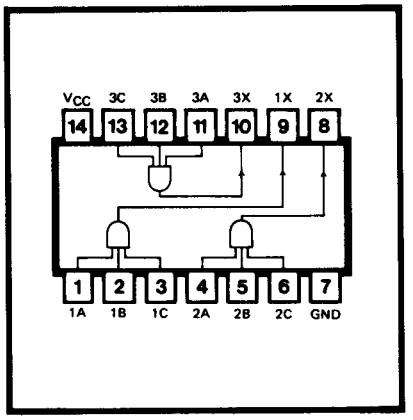

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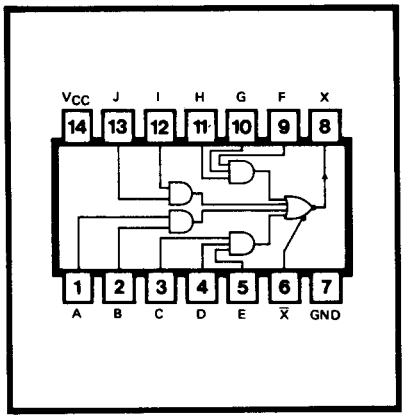

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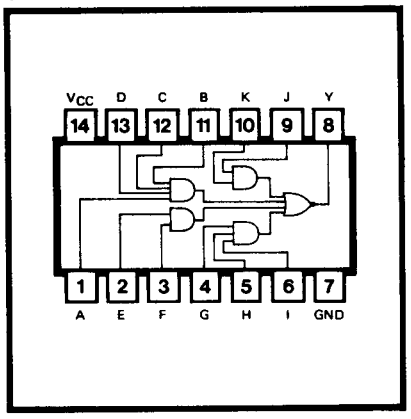

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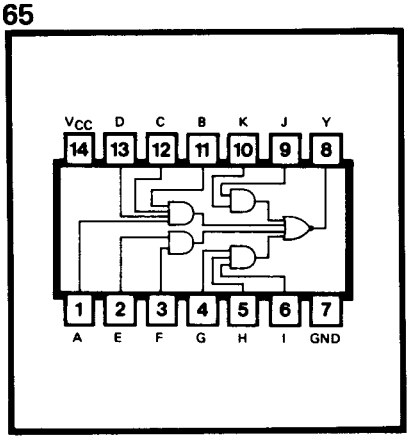

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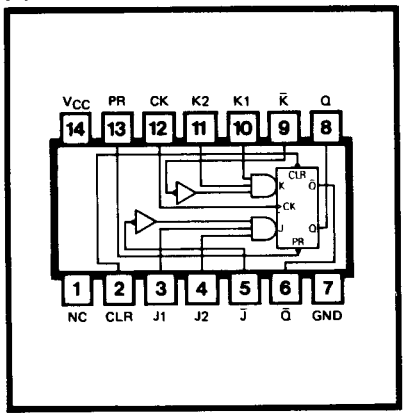

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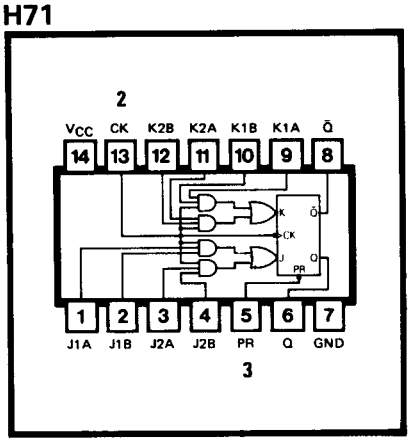

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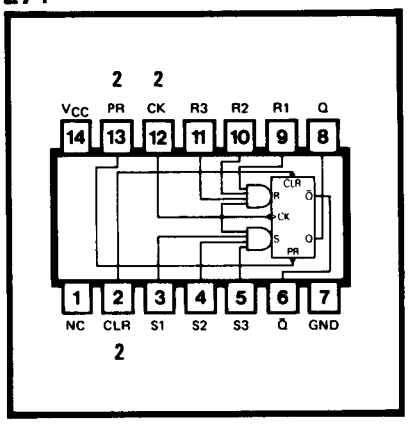

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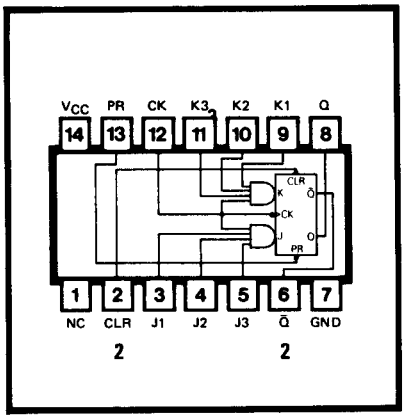

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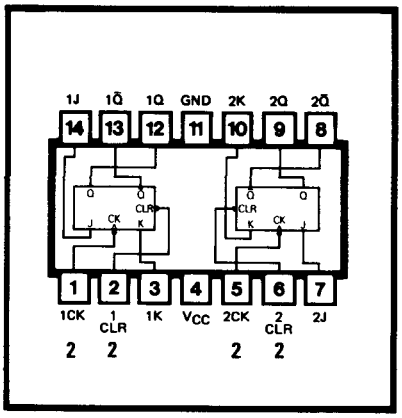

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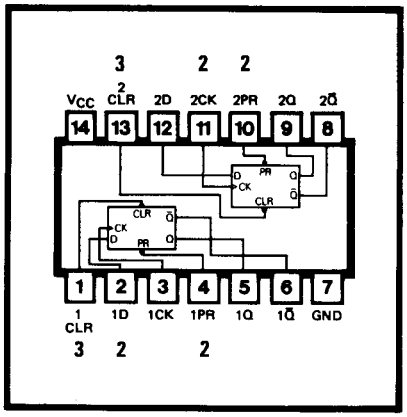

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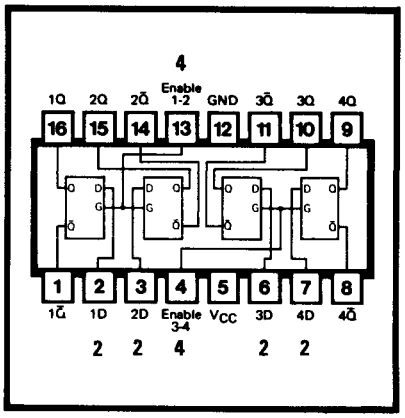

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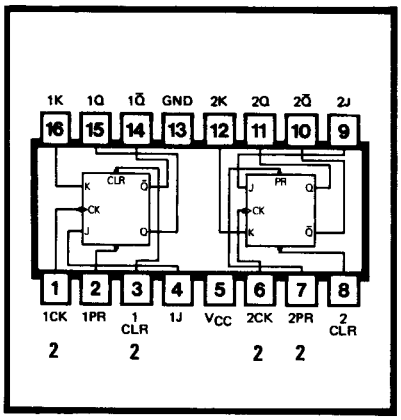

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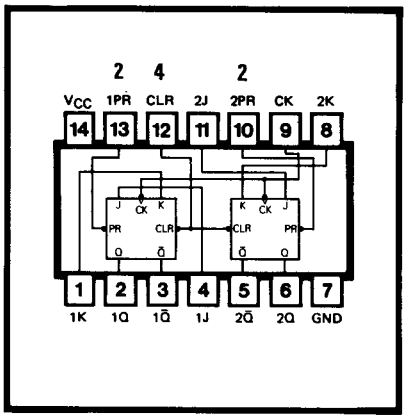

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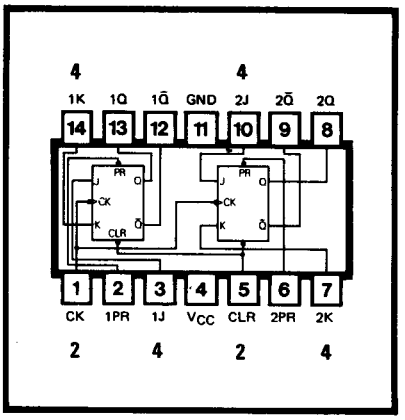

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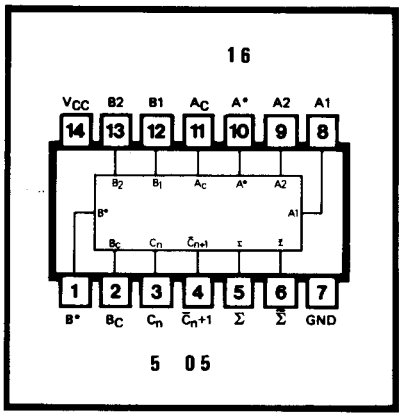

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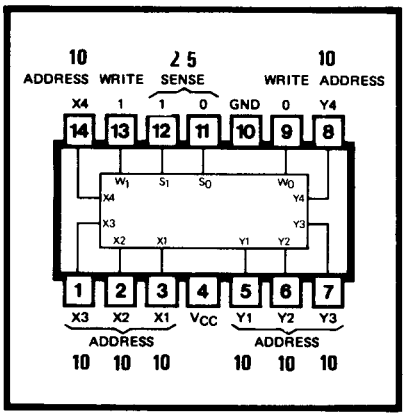

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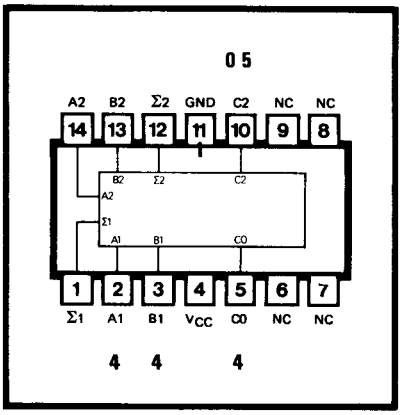

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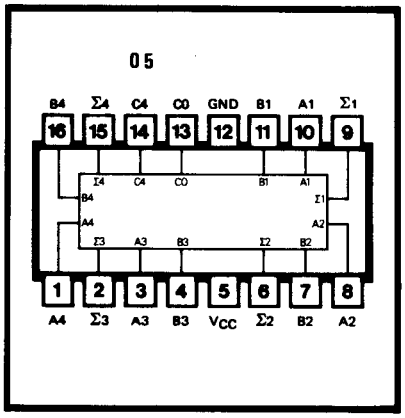

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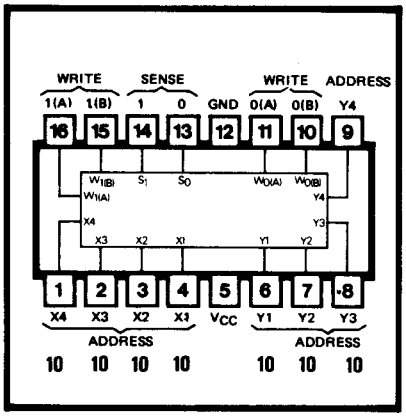

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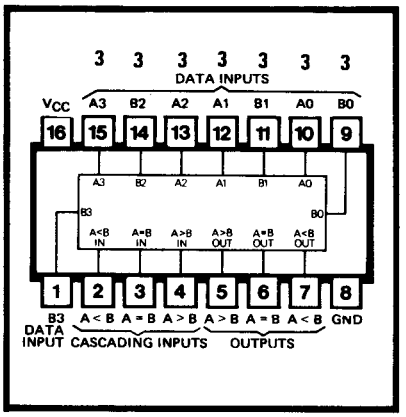
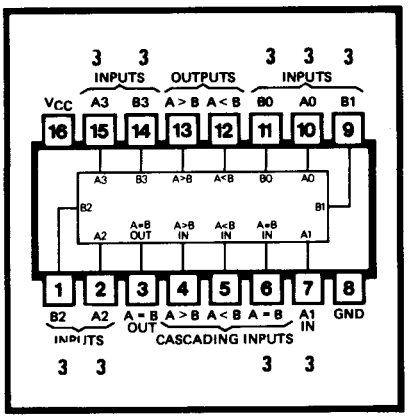


Pin Configuration Guide

L85



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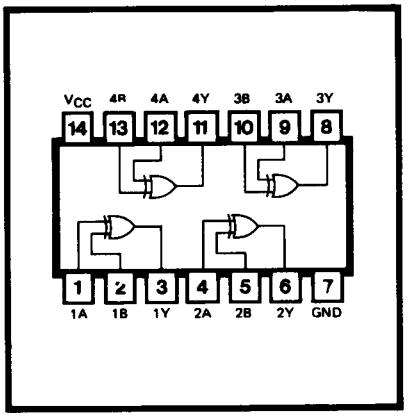

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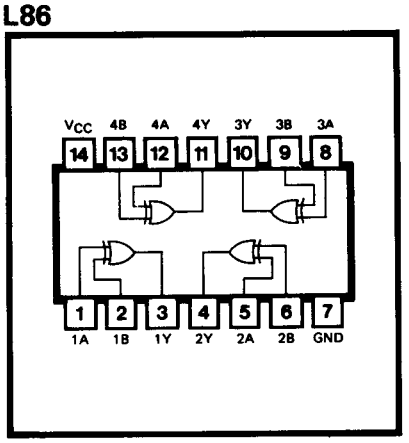

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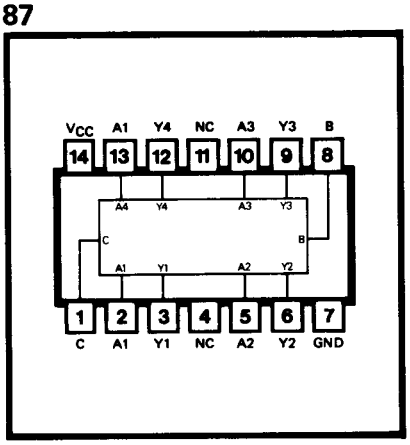

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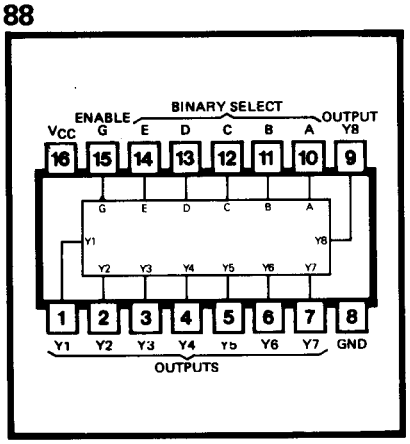

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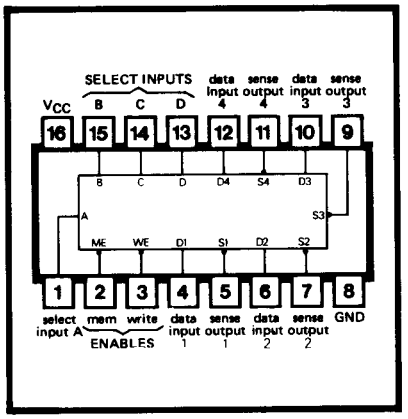

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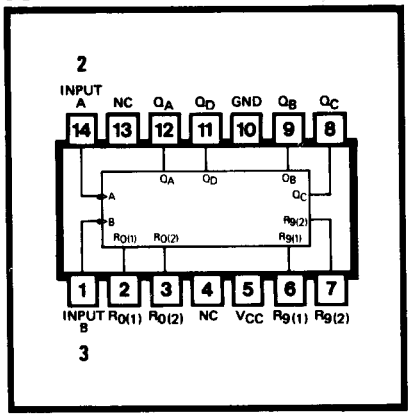

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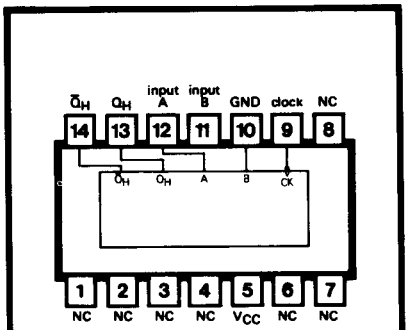

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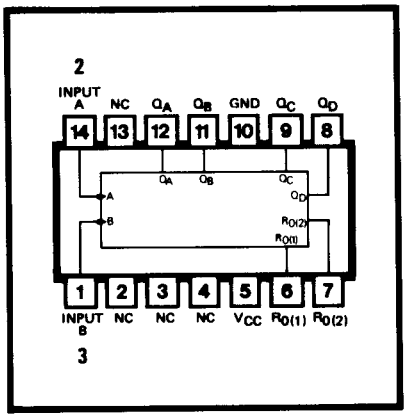

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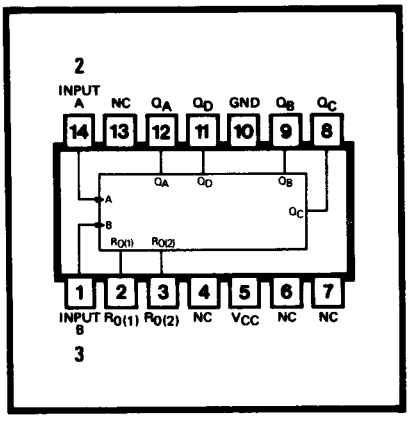

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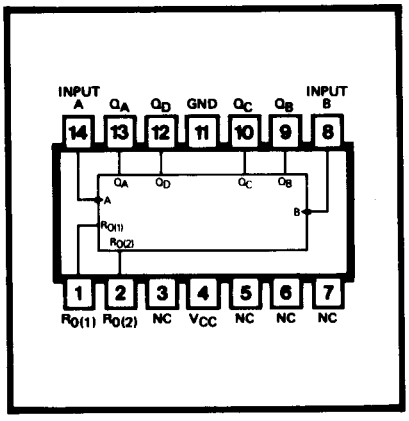

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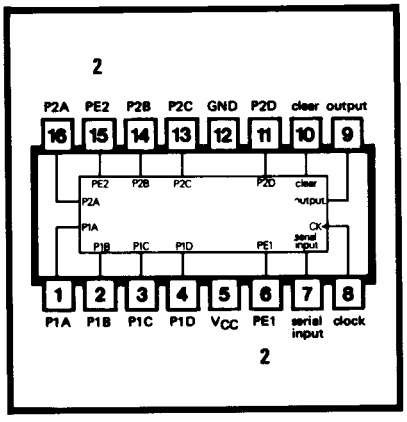

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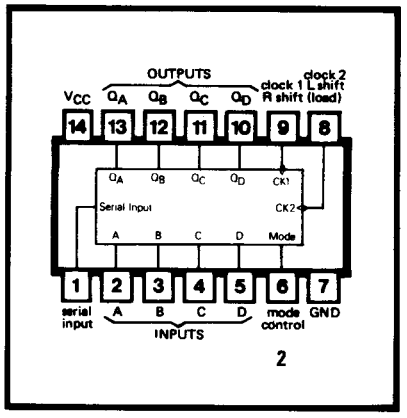

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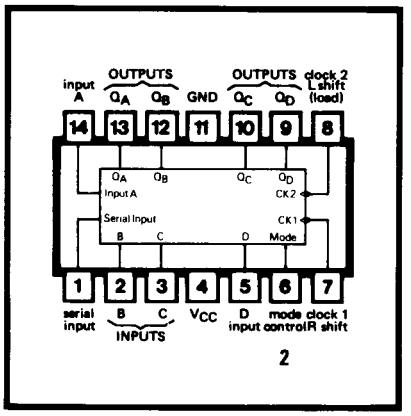

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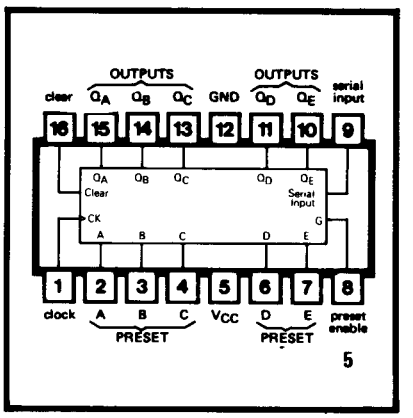

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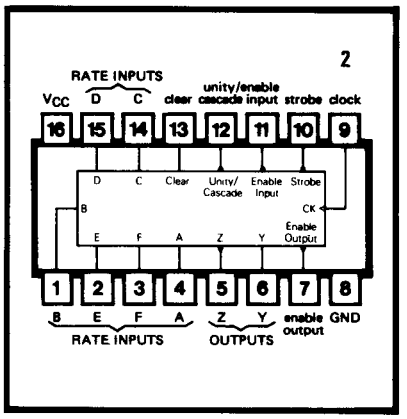

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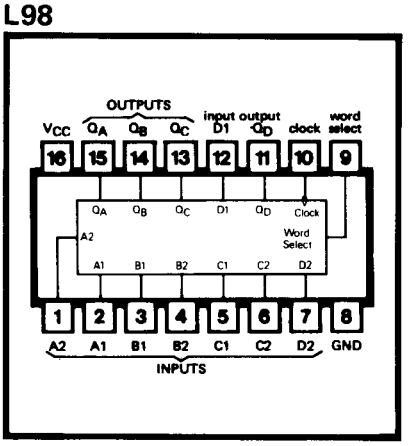

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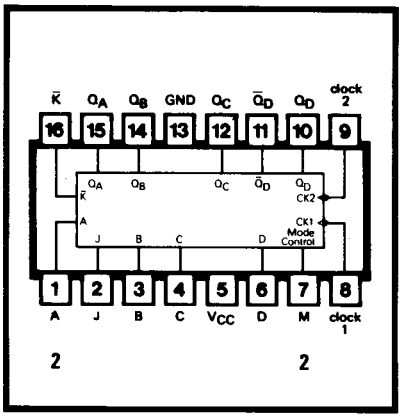

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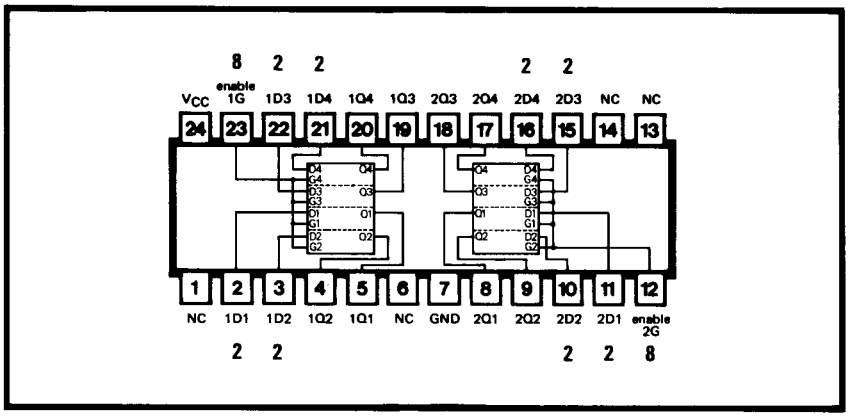

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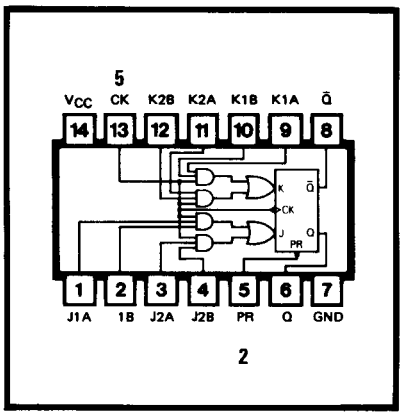

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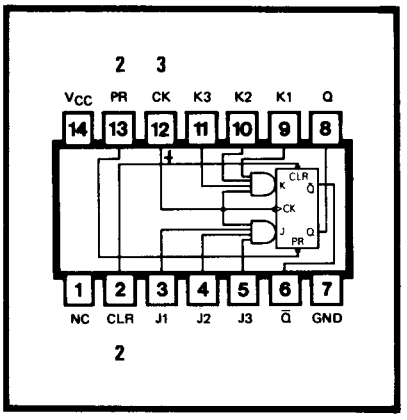

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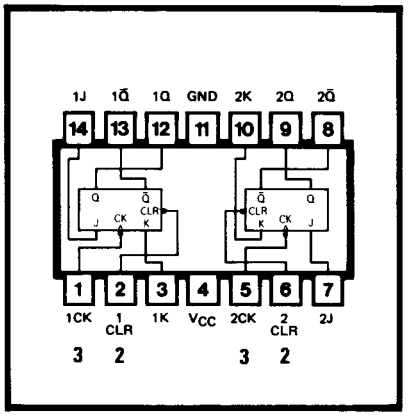

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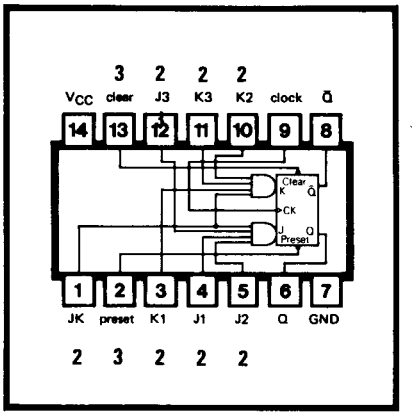

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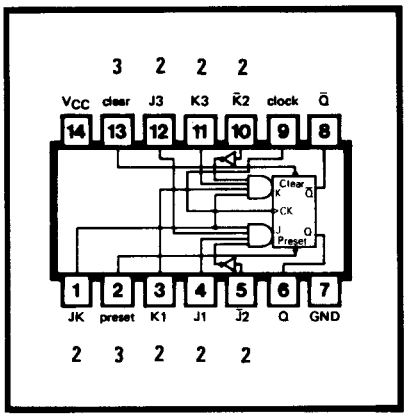

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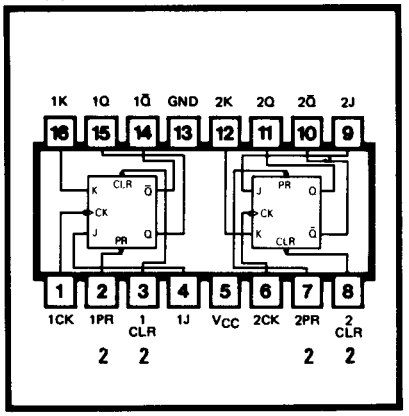

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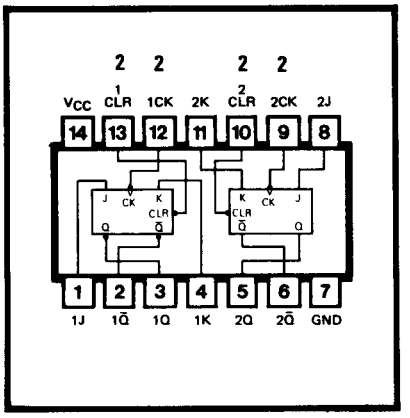

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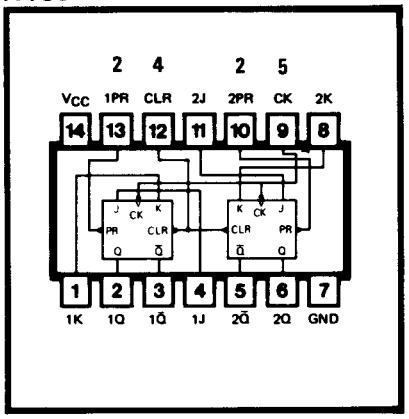

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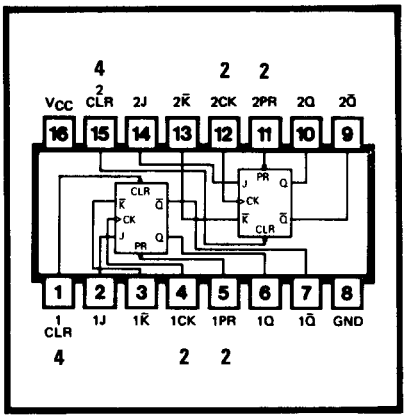

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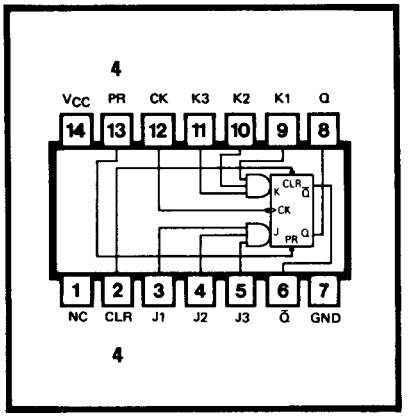

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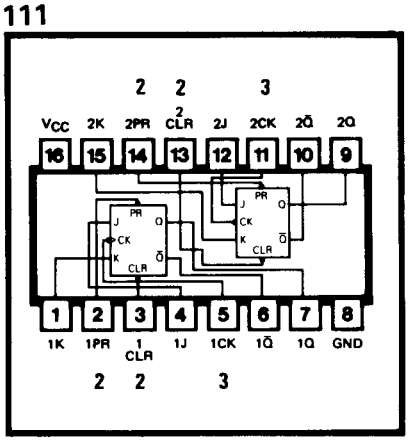

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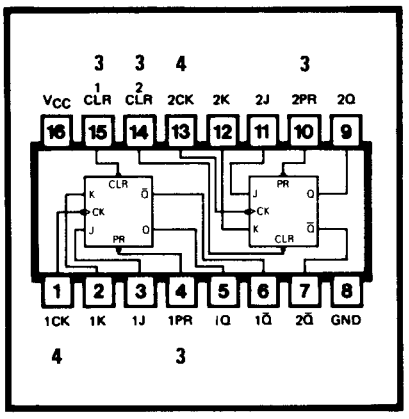

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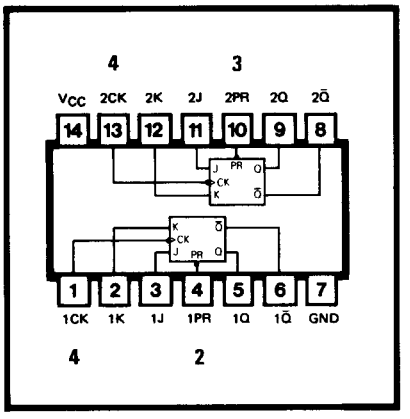

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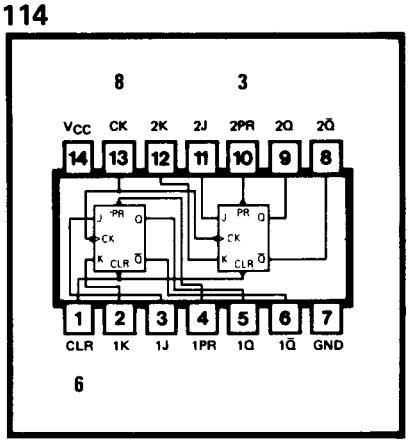

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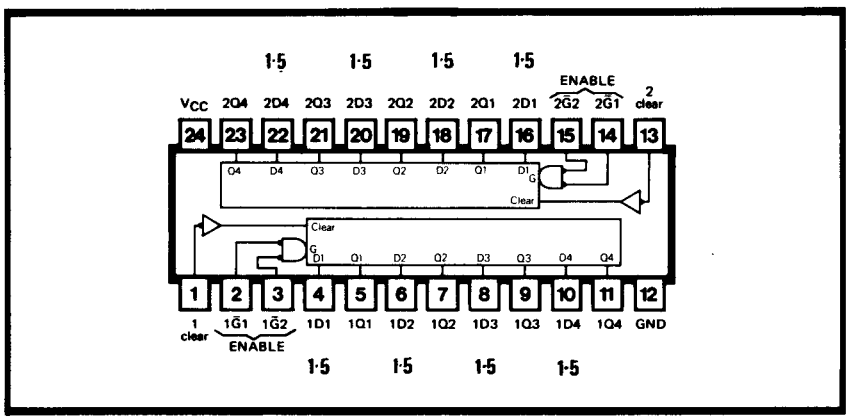

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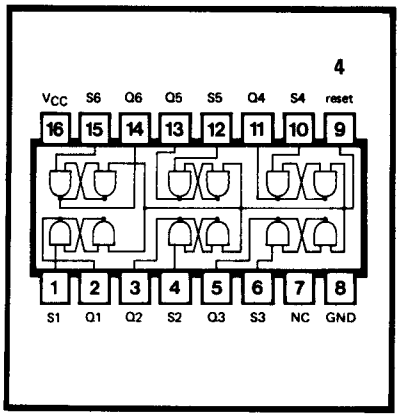

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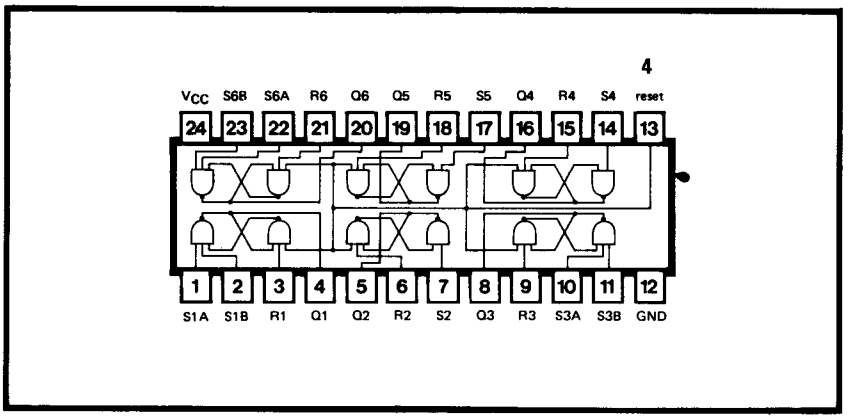

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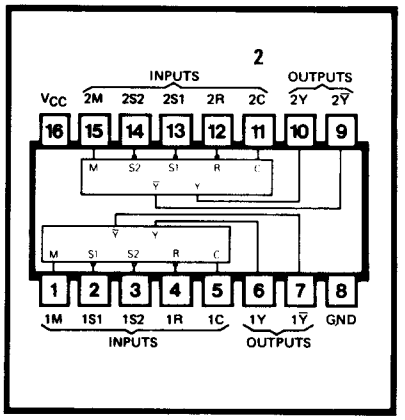

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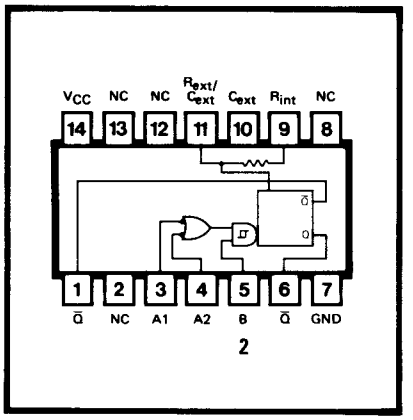

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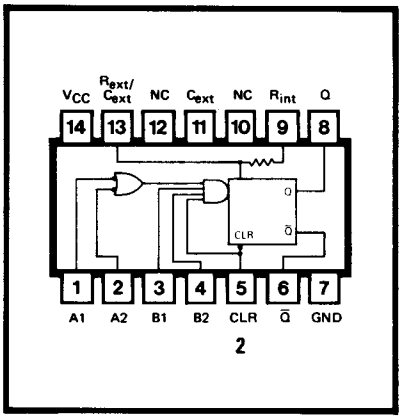

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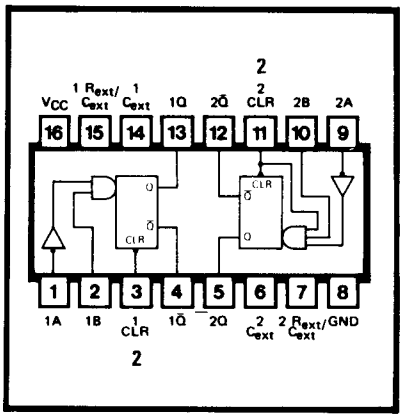

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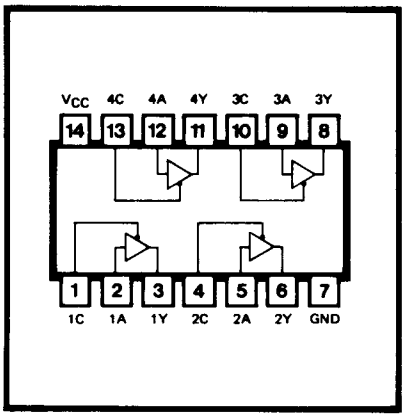

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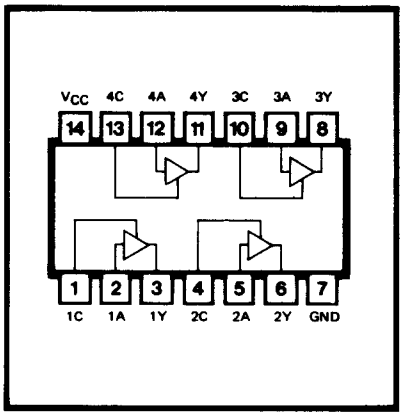

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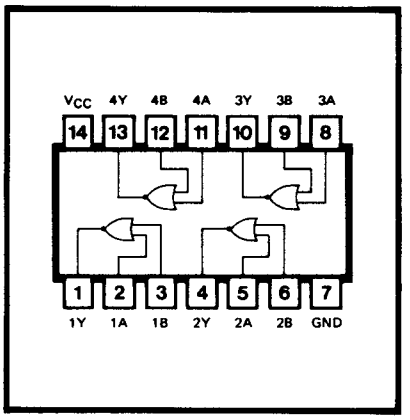

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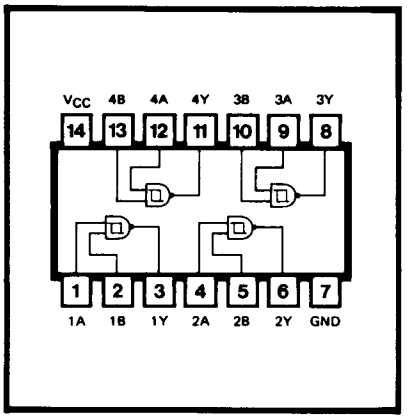

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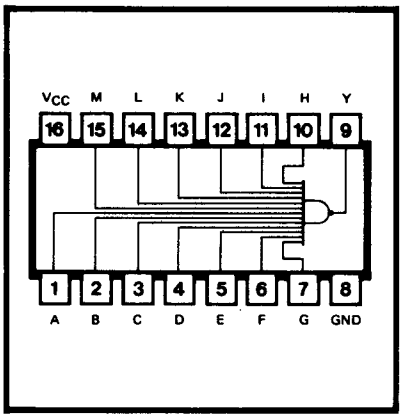

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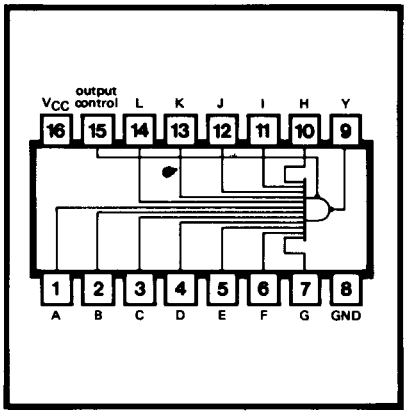

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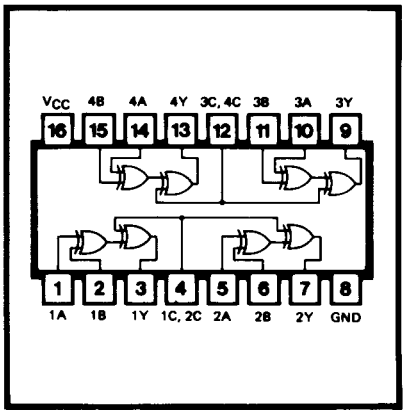

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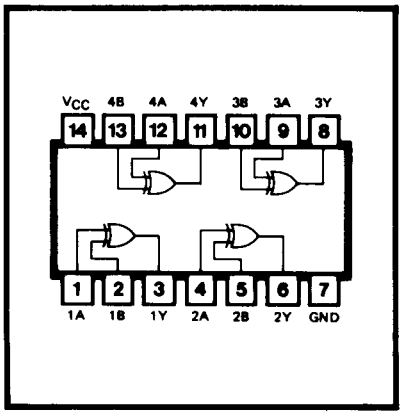

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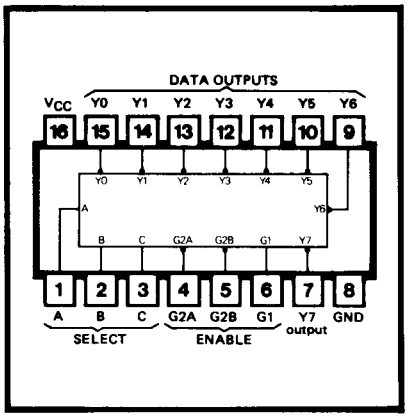

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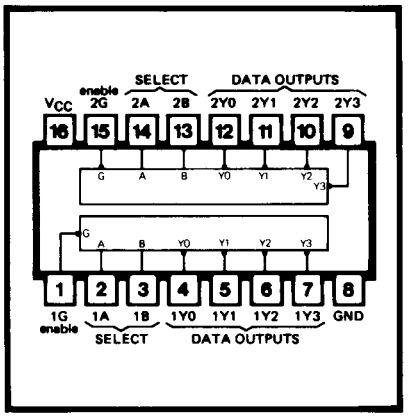

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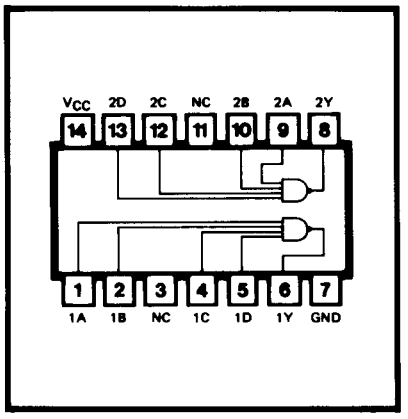

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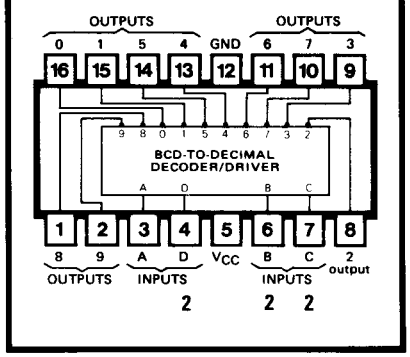

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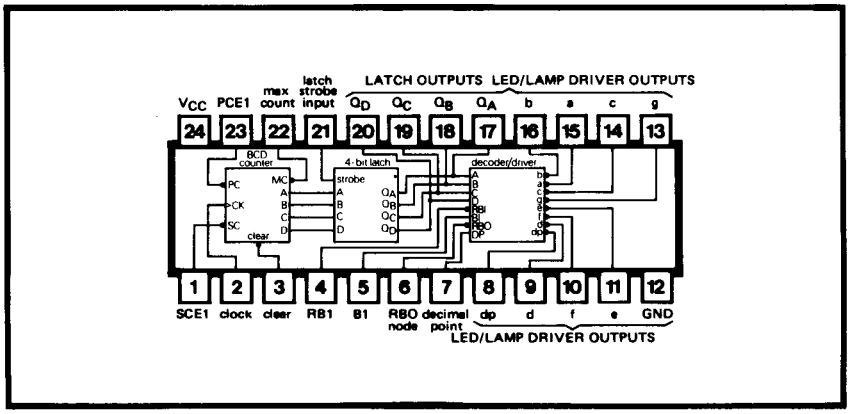

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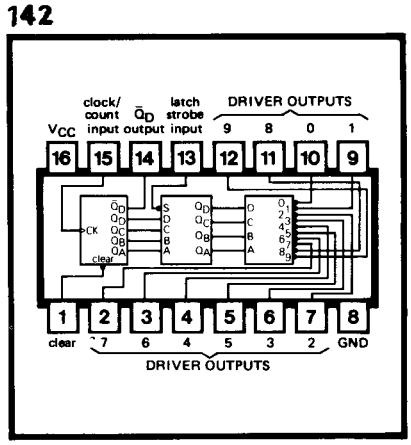

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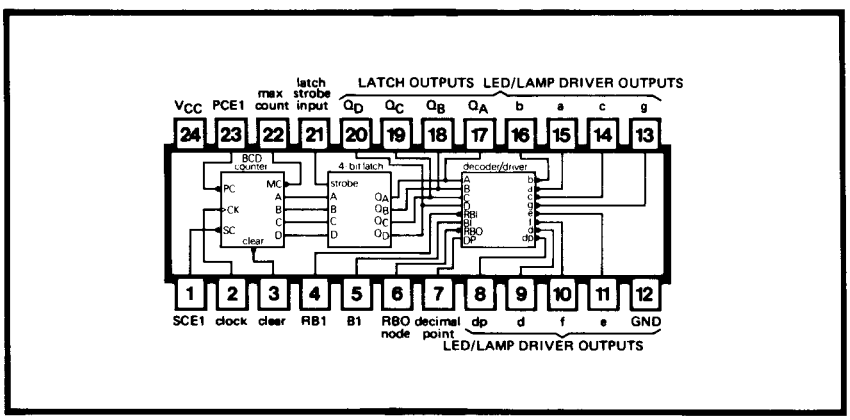

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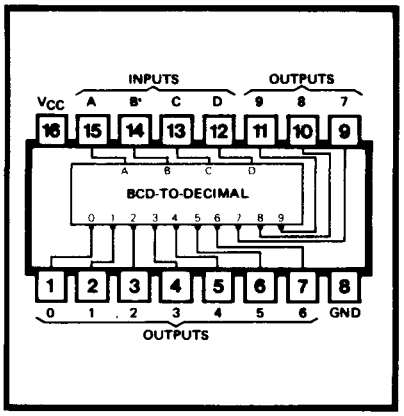

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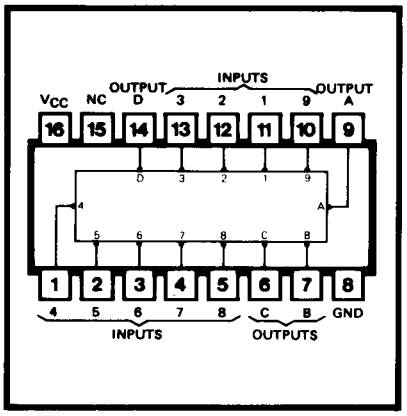

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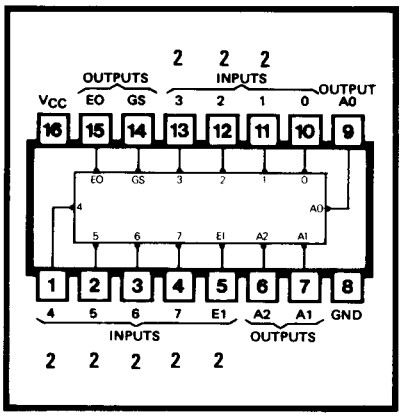

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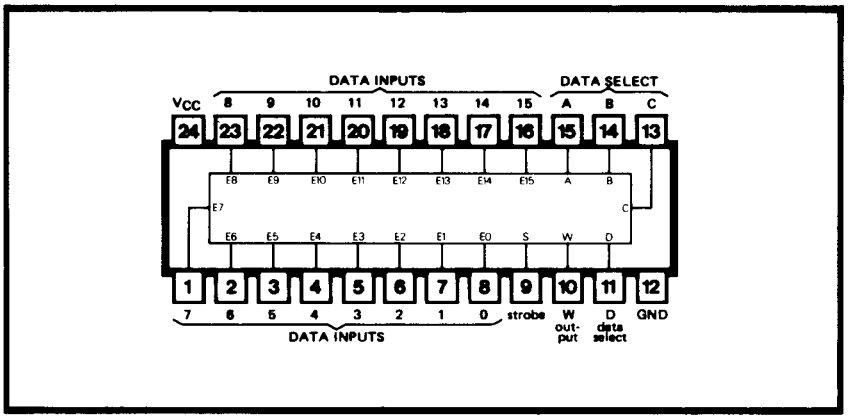

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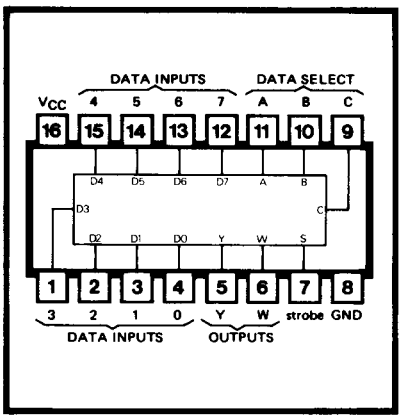

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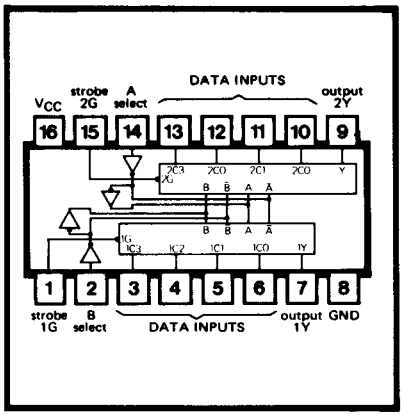

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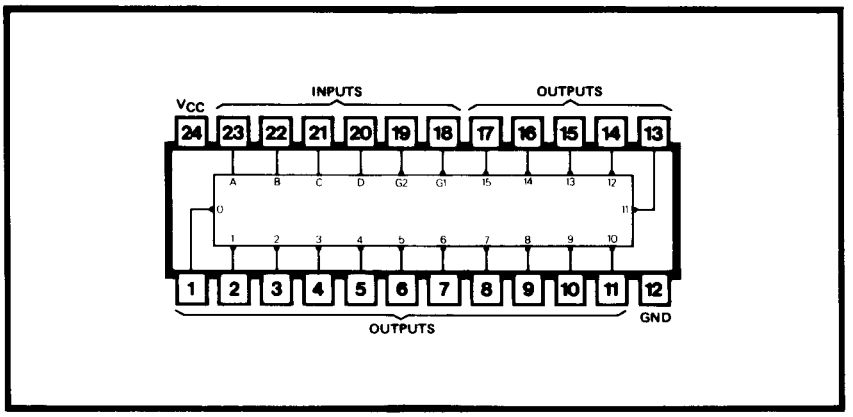

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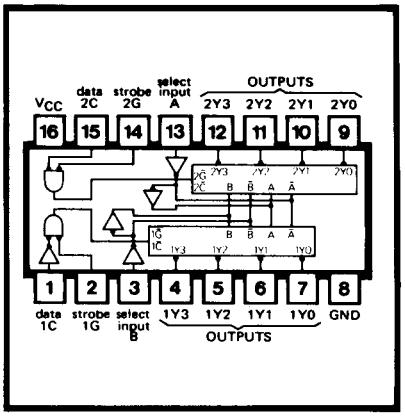

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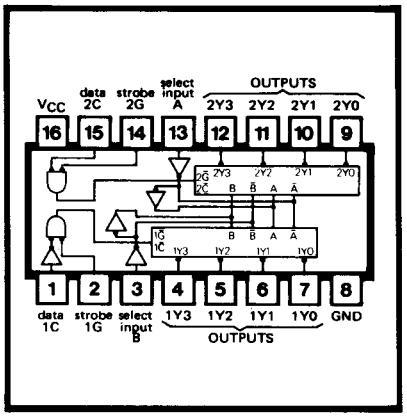

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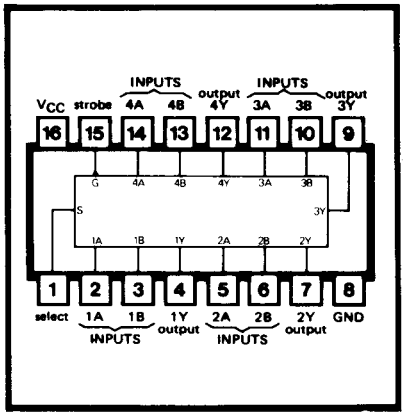

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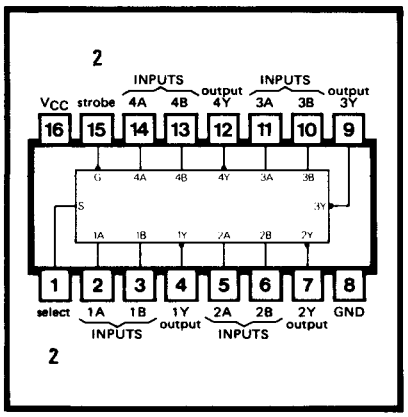

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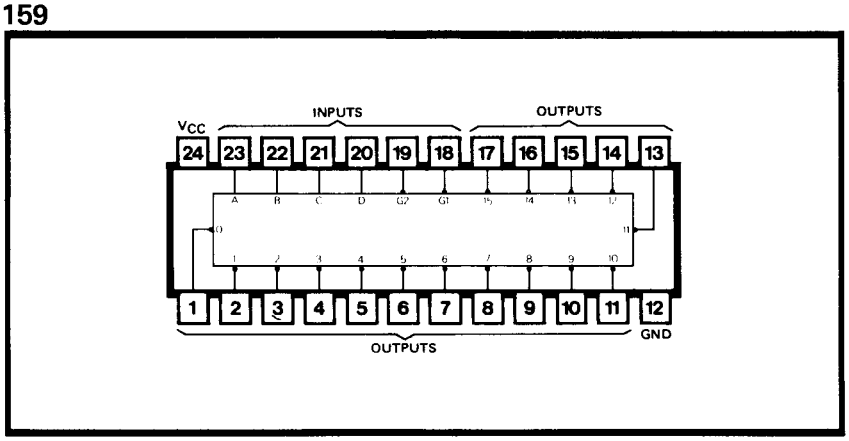

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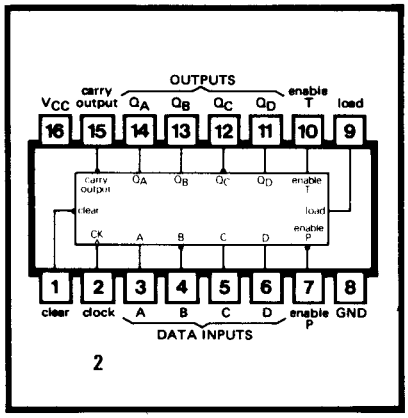

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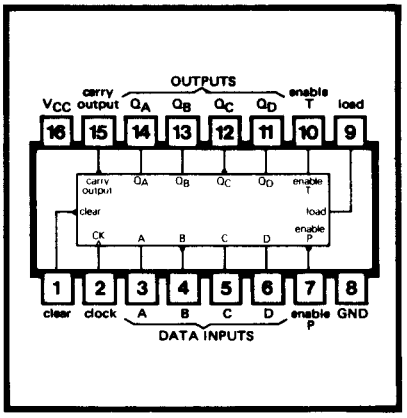

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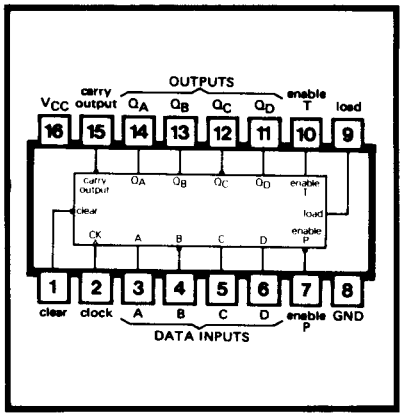

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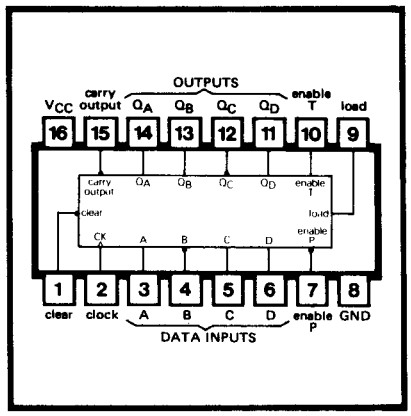

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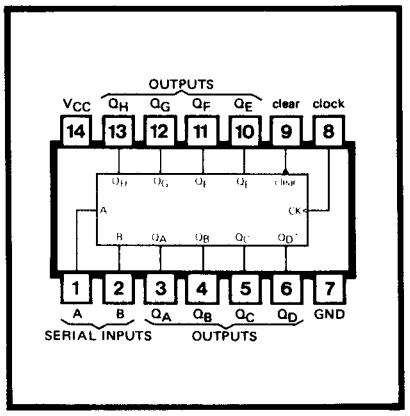

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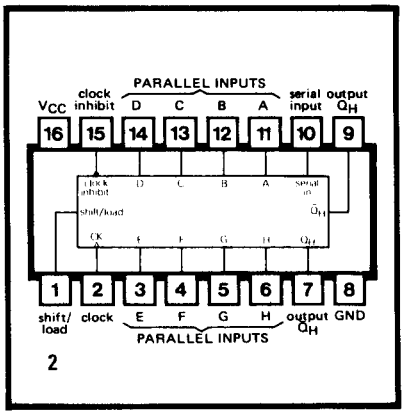

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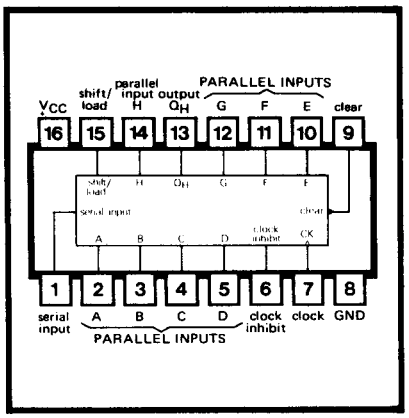

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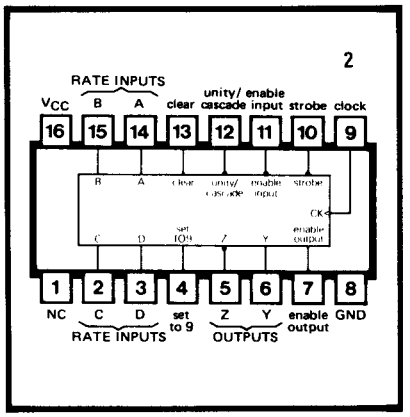

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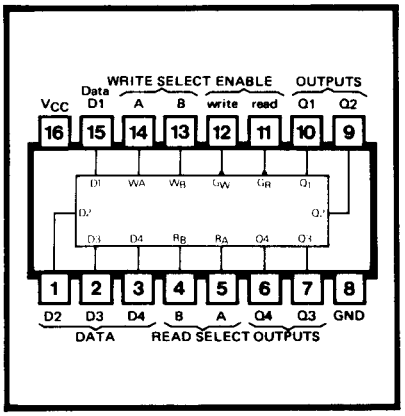

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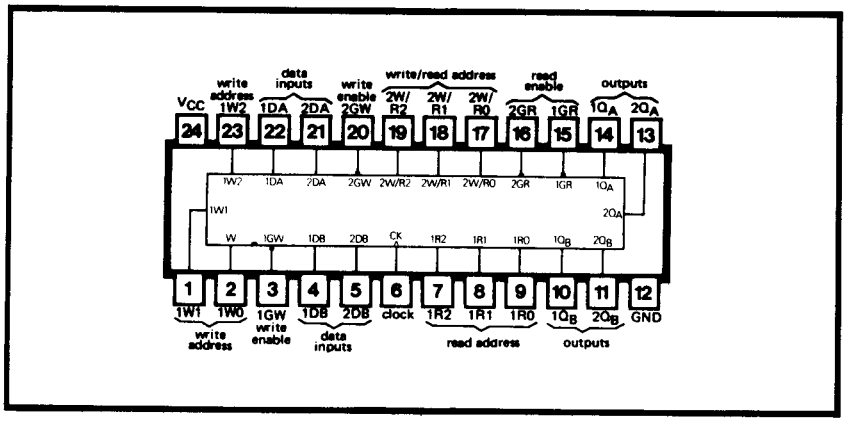

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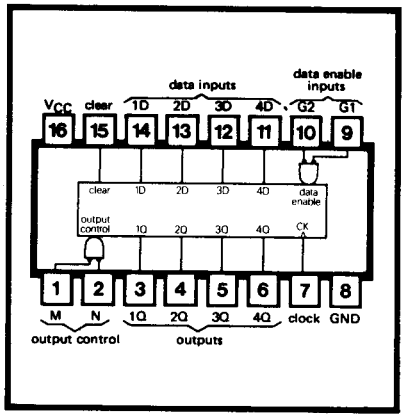

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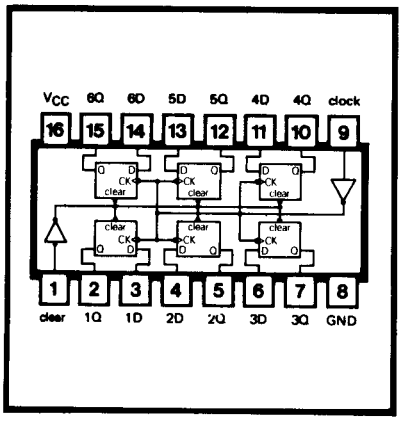

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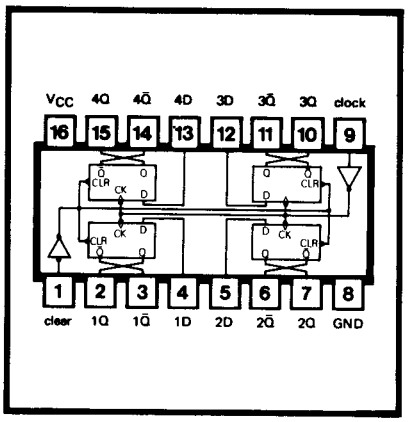

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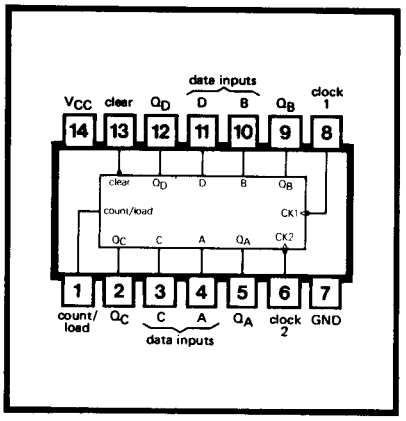

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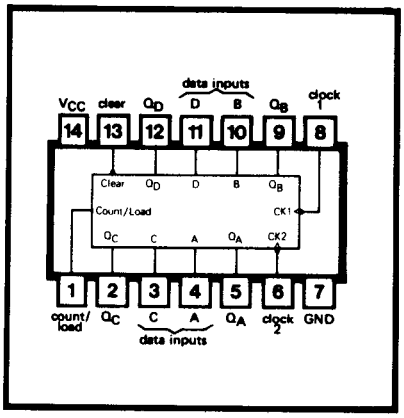

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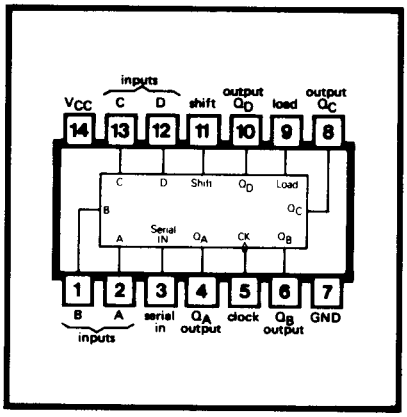

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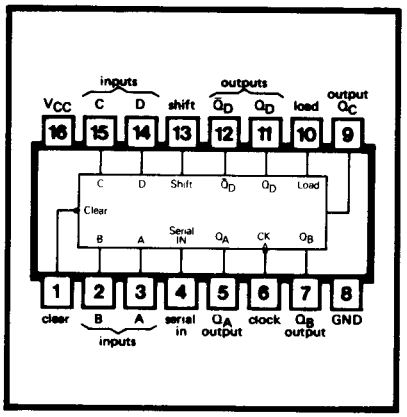

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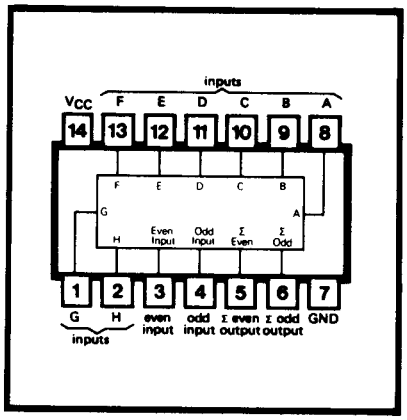

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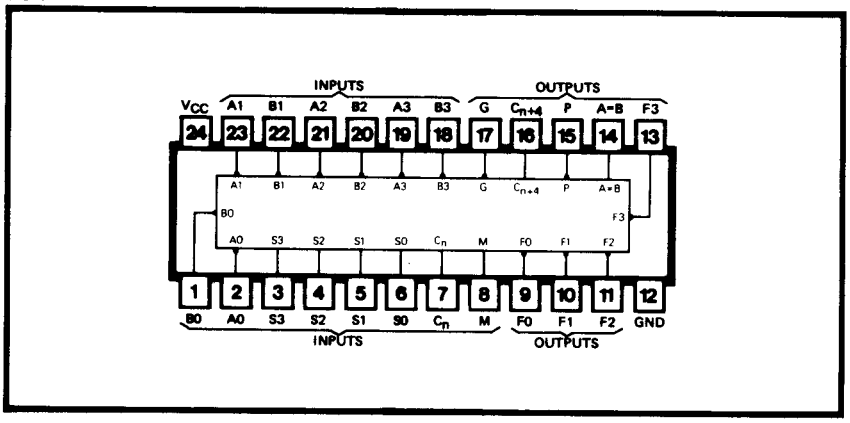

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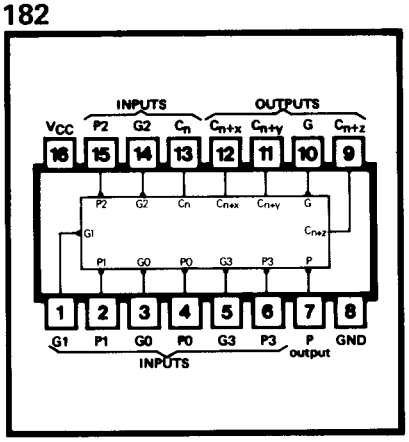

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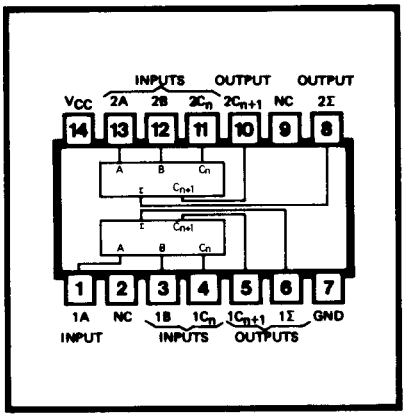

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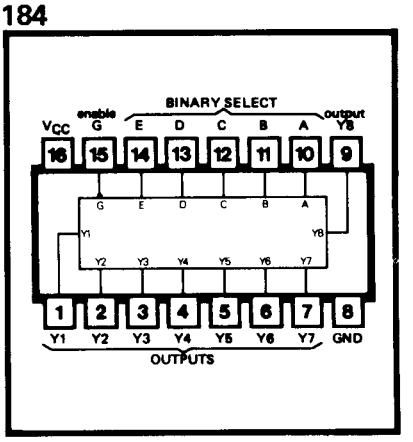

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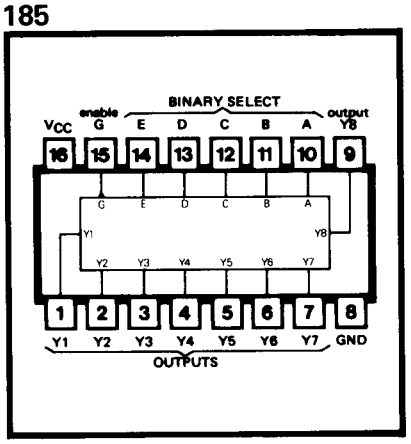

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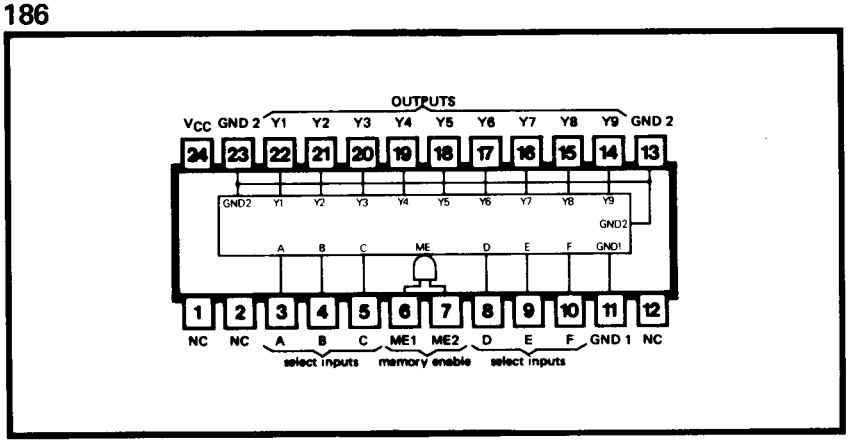

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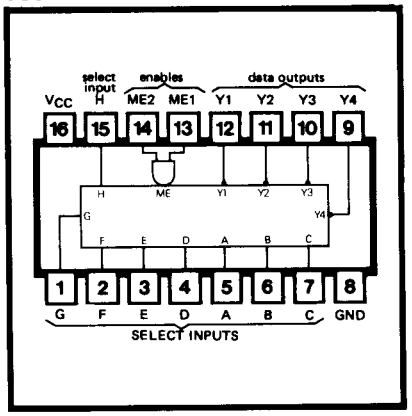

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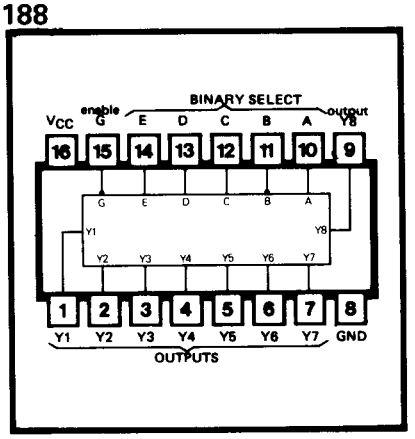

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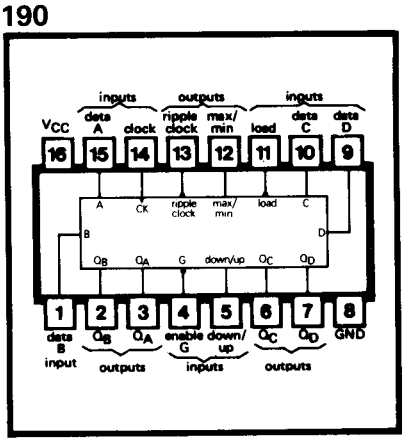

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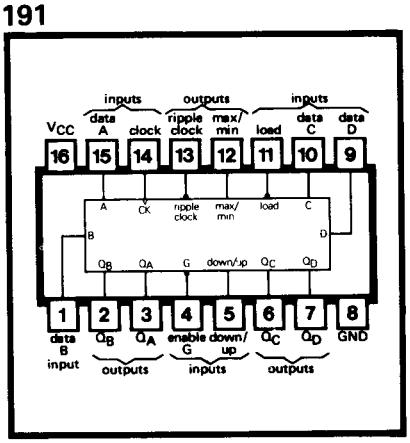

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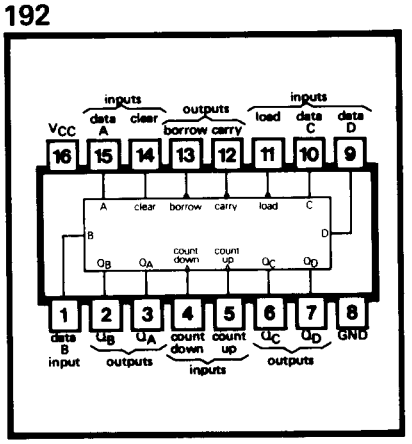

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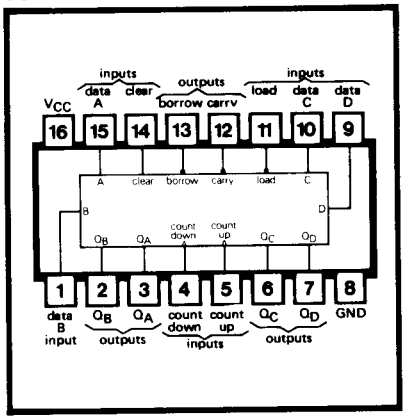

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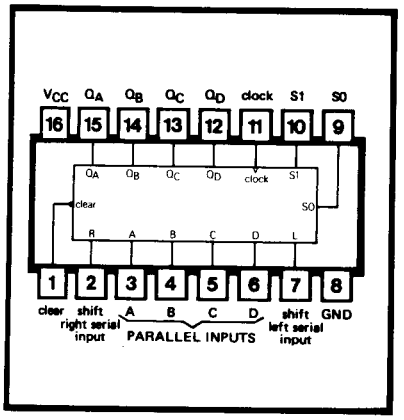

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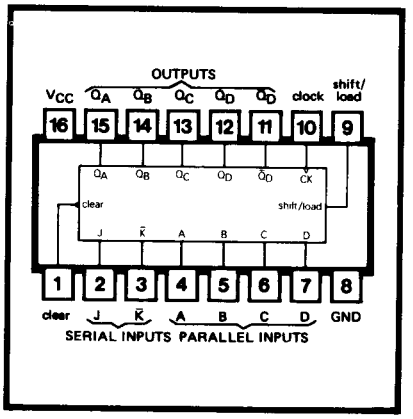

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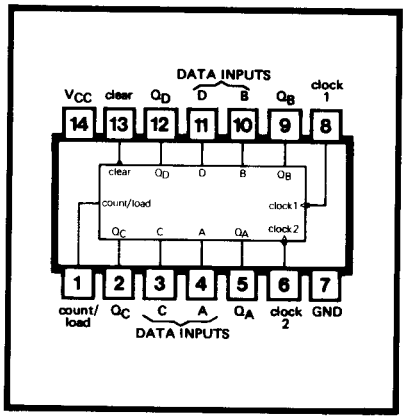

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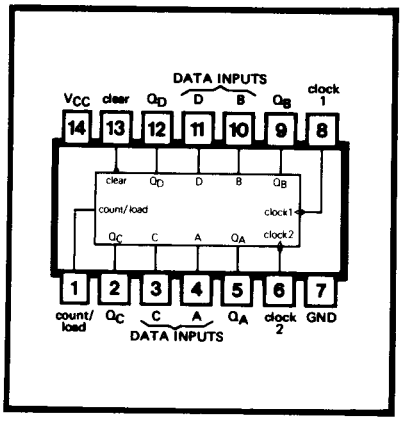

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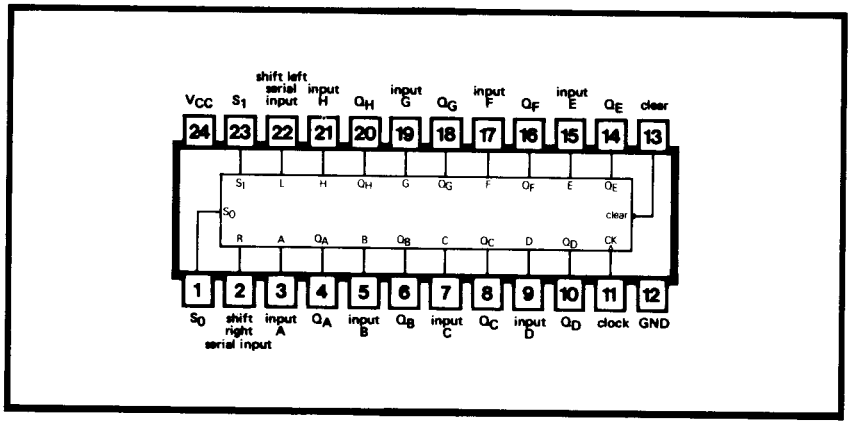

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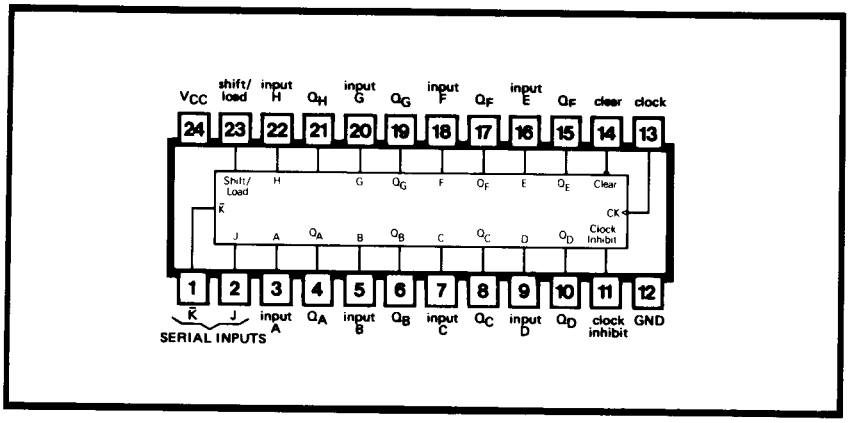

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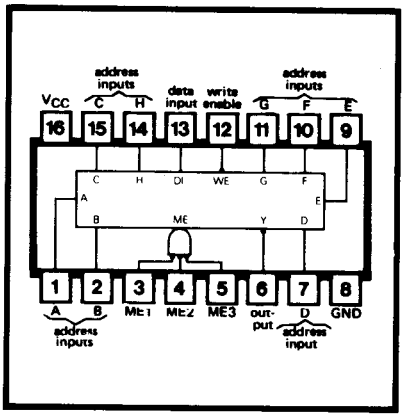

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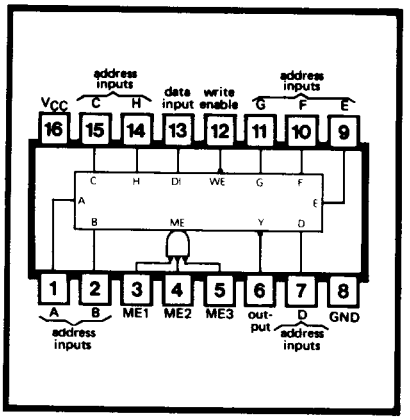

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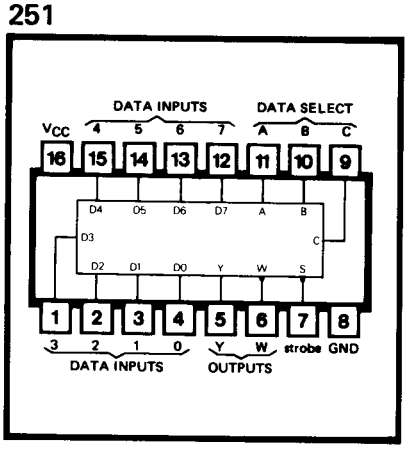

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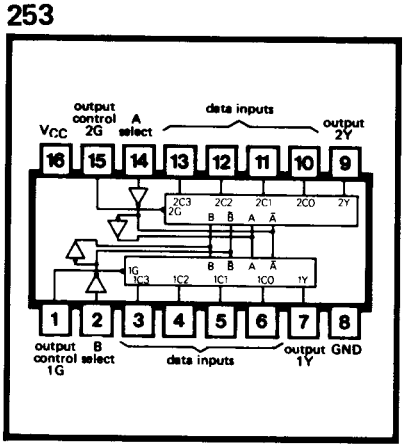

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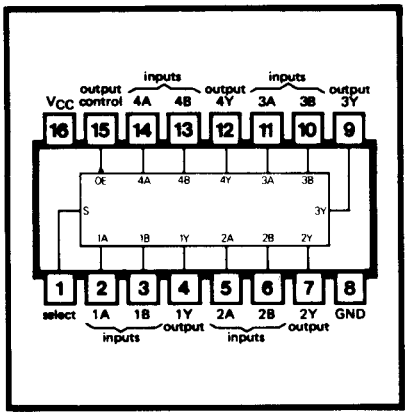

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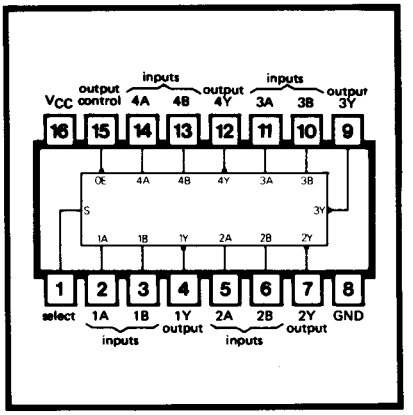

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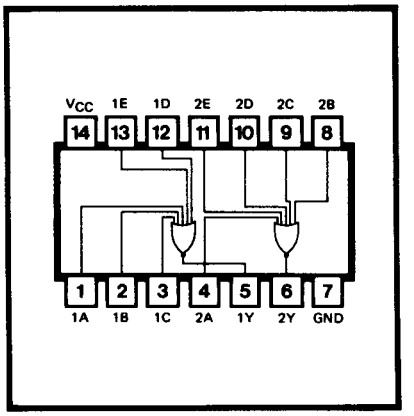

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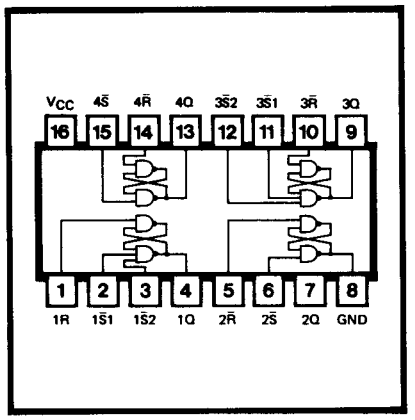

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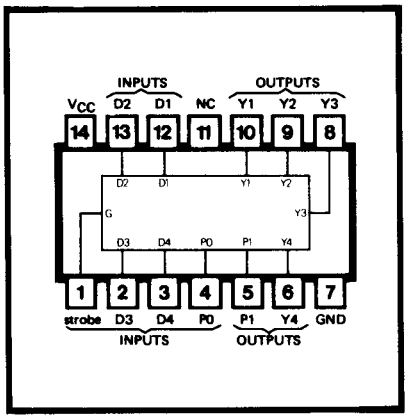

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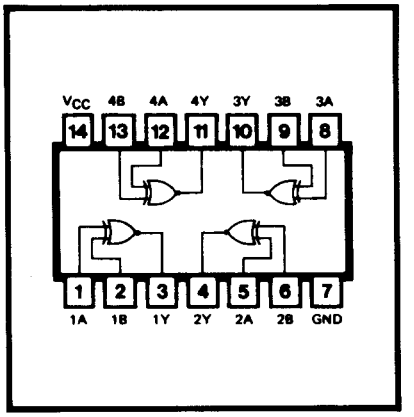

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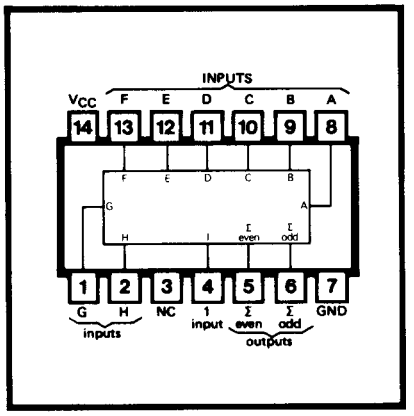

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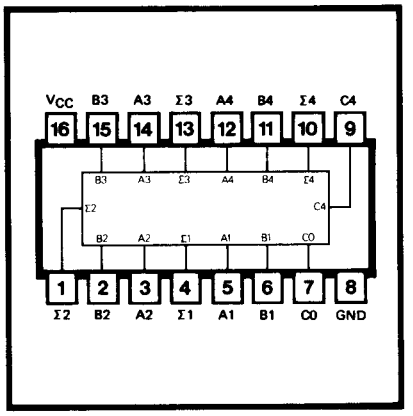

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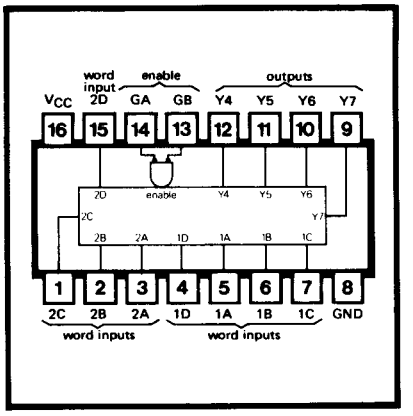

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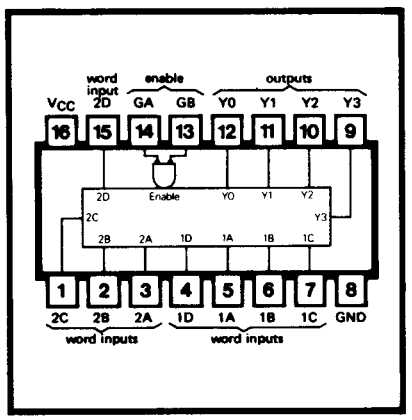

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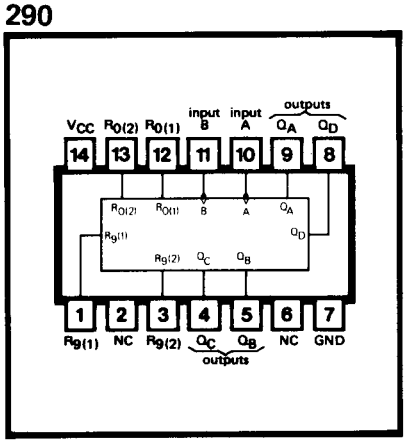

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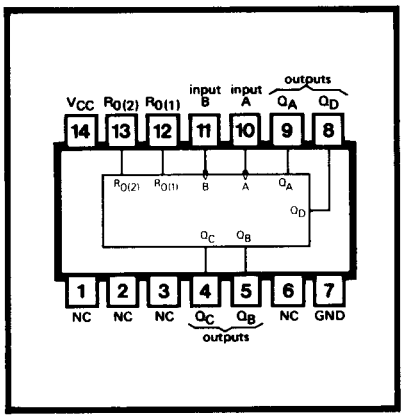

PIN CONFIGURATION GUIDE

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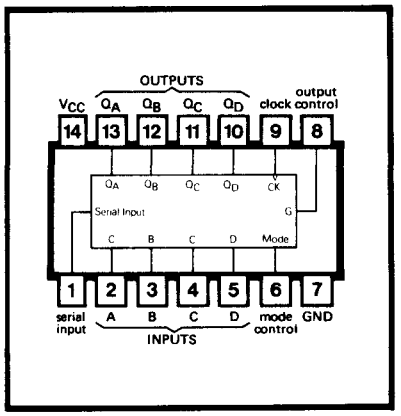

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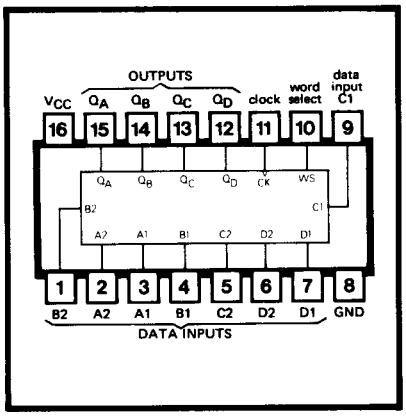
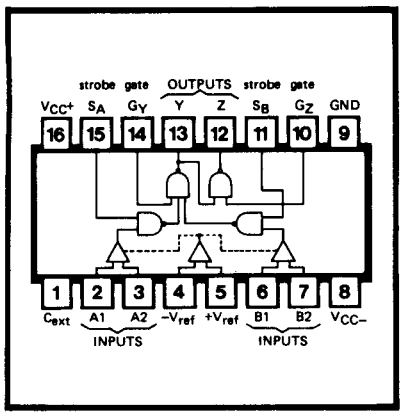


SYSTEM 74 INTERFACE CIRCUITS

SN7520



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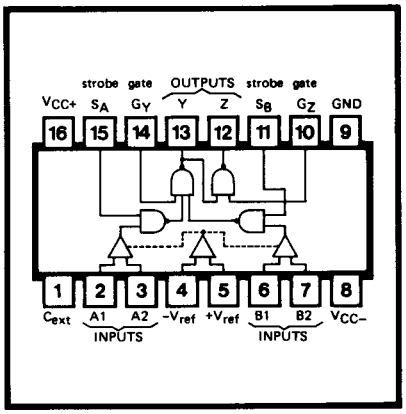

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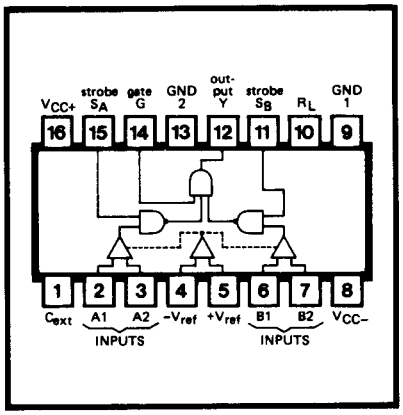

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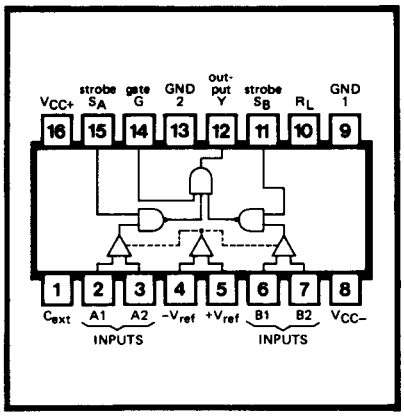

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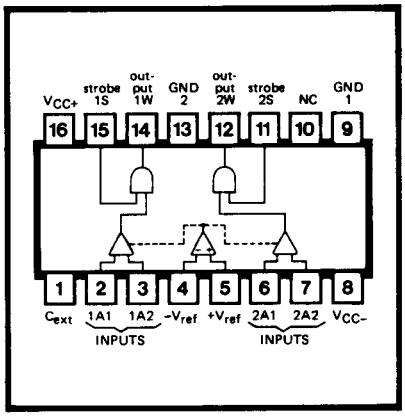

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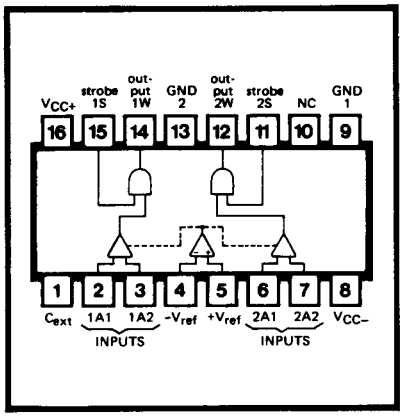
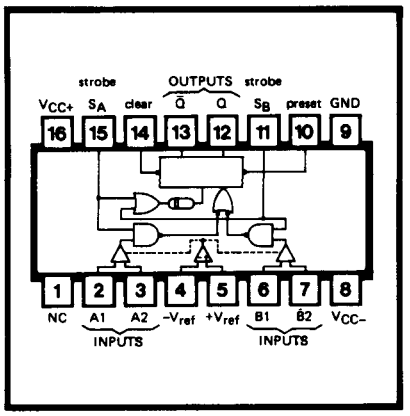


Pin Configuration Guide

SN7526



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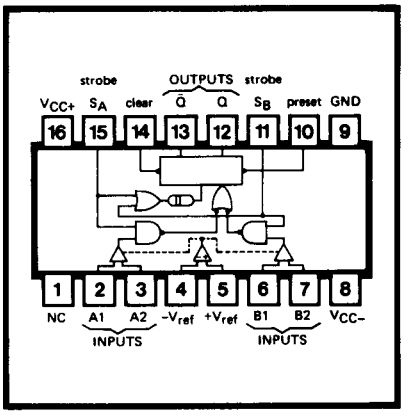

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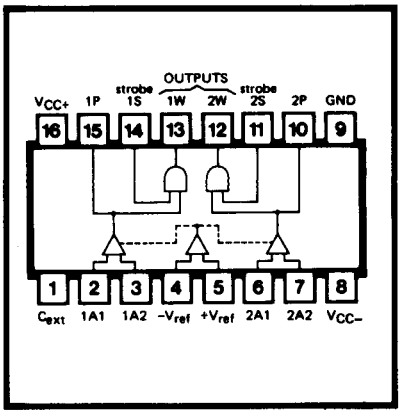

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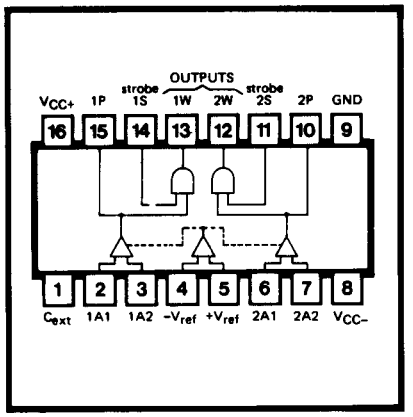

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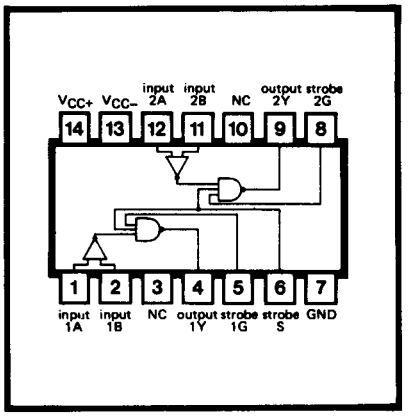

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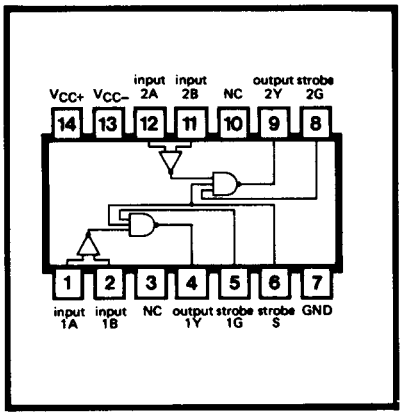

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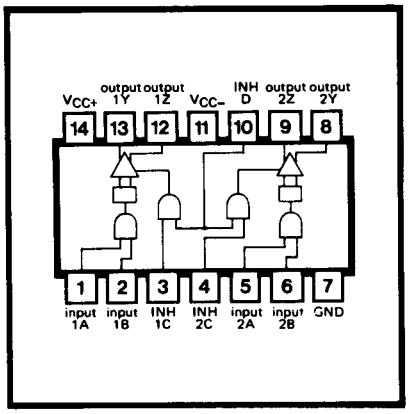

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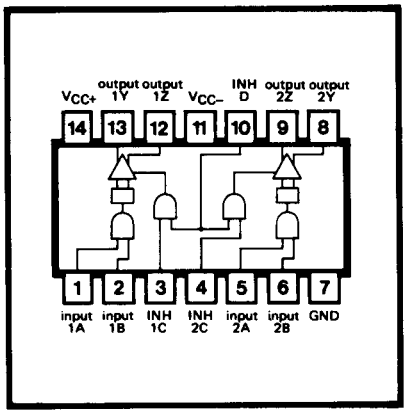

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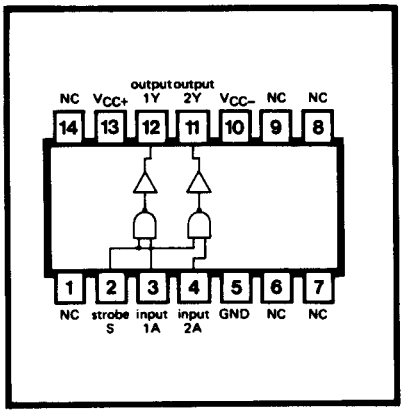

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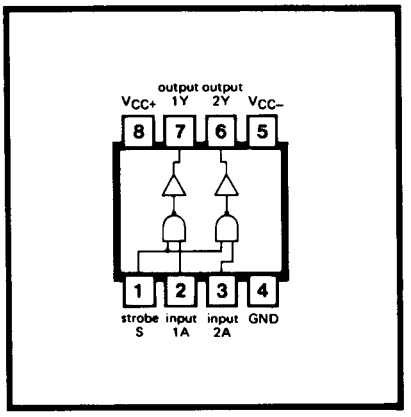

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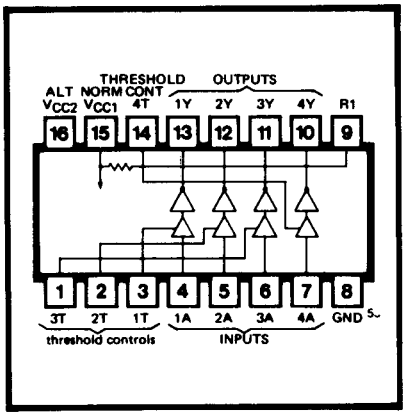

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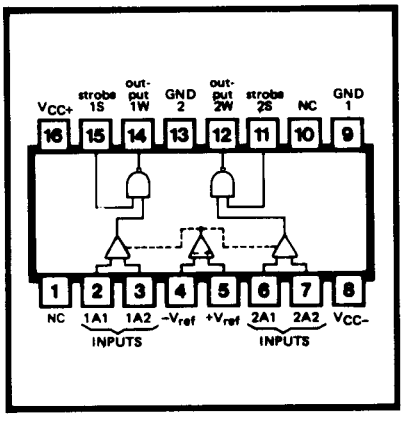
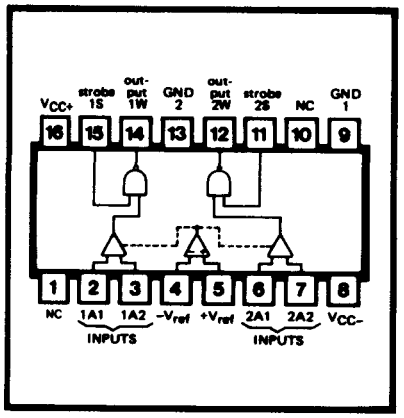


PIN CONFIGURATION GUIDE

SN75235



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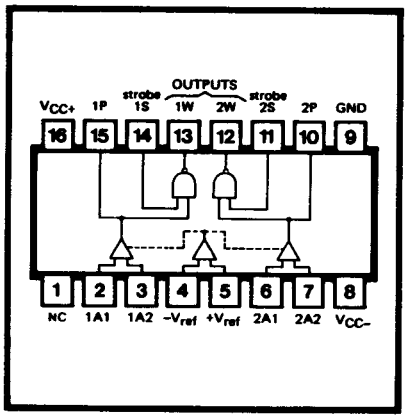

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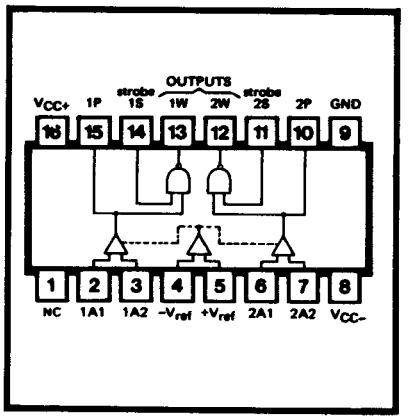

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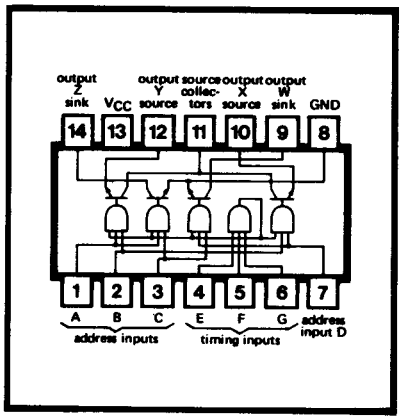

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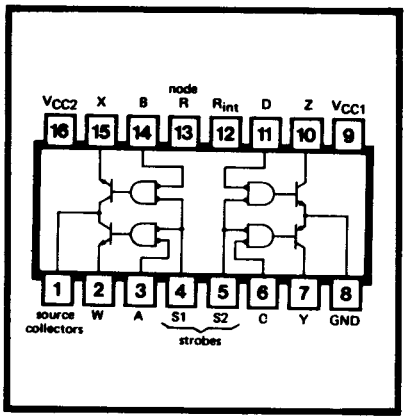

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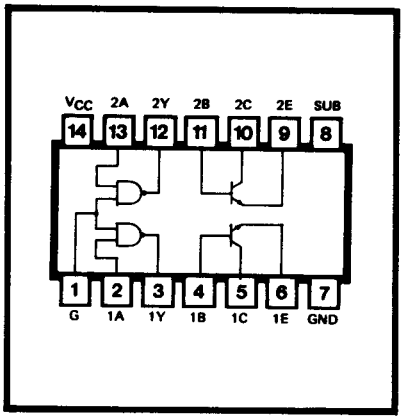

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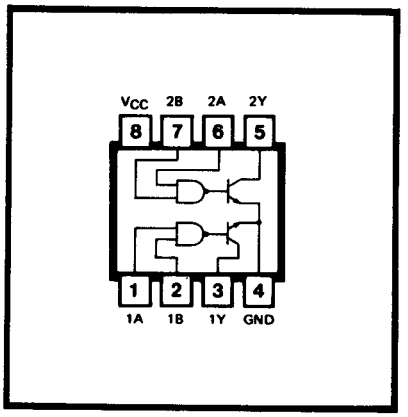

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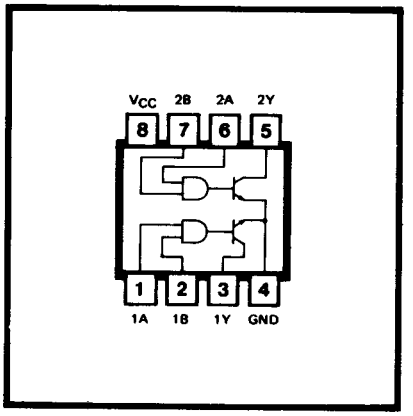

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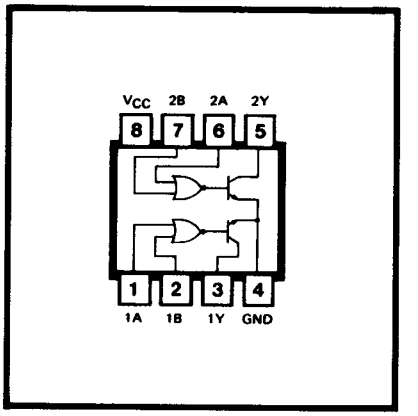

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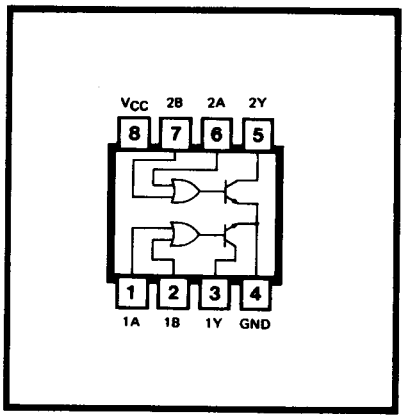


Applications of TTL Logic

Gates

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
HEX INVERTERS	3 ns 6 ns 9.5 ns 10 ns 33 ns	19 mW 22 mW 2 mW 10 mW 1 mW	SN74S04 SN74H04 SN74LS04 SN7404 SN74L04
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	3 ns 6 ns 9.5 ns 10 ns 33 ns	19 mW 22 mW 2 mW 10 mW 1 mW	SN74S00 SN74H00 SN74LS00 SN7400 SN74L00
TRIPLE 3-INPUT POSITIVE-NAND GATES	3 ns 6 ns 9.5 ns 10 ns 33 ns	19 mW 22 mW 2 mW 10 mW 1 mW	SN74S10 SN74H10 SN74LS10 SN7410 SN74L10
DUAL 4-INPUT POSITIVE-NAND GATES	3 ns 6 ns 9.5 ns 10 ns 33 ns	19 mW 22 mW 2 mW 10 mW 1 mW	SN74S20 SN74H20 SN74LS20 SN7420 SN74L20
8-INPUT POSITIVE-NAND GATES	3 ns 6 ns 17 ns 10 ns 33 ns	19 mW 22 mW 2 mW 10 mW 1 mW	SN74S30 SN74H30 SN74LS30 SN7430 SN74L30
13-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN74S133

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
HEX INVERTERS	5 ns 8 ns 16 ns 22 ns	17.5 mW 22 mW 2 mW 10 mW	SN74S05 SN74H05 SN74LS05 SN7405
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	5 ns 8 ns 16 ns 16 ns 22 ns 22 ns 41 ns	17,5 mW 22 mW 2 mW 2 mW 10 mW 10 mW 1 mW	SN74S03 SN74H01 SN74LS01 SN74LS03 SN7401 SN7403 SN74L03
TRIPLE 3-INPUT POSITIVE-NAND GATES	22 ns	10 mW	SN7412
DUAL 4-INPUT POSITIVE-NAND GATES	5 ns 8 ns 16 ns 22 ns	17,5 mW 22 mW 2 mW 10 mW	SN74S22 SN74H22 SN74LS22 SN7422

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-AND GATES	12 ns 15 ns	4.25 mW 19 mW	SN74LS08 SN7408
TRIPLE 3-INPUT POSITIVE-AND GATES	4.75 ns 8.2 ns 12 ns	31 mW 40 mW 4.25 mW	SN74S11 SN74H11 SN74LS11
DUAL 4-INPUT POSITIVE-AND GATES	8.2 ns 12 ns	40 mW 4.25 mW	SN74H21 SN74LS21

POSITIVE AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-AND GATES	18.5 ns 20 ns	19.4 mW 4.25 mW	SN7409 SN74LS09
TRIPLE 3-INPUT POSITIVE-AND GATES	6 ns 10.5 ns 20 ns	28 mW 38 mW 4.25 mW	SN74S15 SN74H15 SN74LS15

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-OR GATES	12 ns 12 ns	24 mW 5 mW	SN7432 SN74LS32

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-NOR GATES	3.5 ns 10 ns 10 ns 33 ns	29 mW 2.75 mW 14 mW 1.5 mW	SN74S02 SN74LS02 SN7402 SN74L02
TRIPLE 3-INPUT POSITIVE-NOR GATES	8.5 ns 10 ns	22 mW 4.5 mW	SN7427 SN74LS27
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN7425
DUAL 5-INPUT POSITIVE-NOR GATES	3.5 ns	29 mW	SN74S260

AND-OR-INVERT GATES WITH TOTEM POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
2-WIDE 4-INPUT	12.5 ns 43 ns	2.75 mW 1.5 mW	SN74LS55 SN74L55
4-WIDE 4-2-3-2-INPUT 4-WIDE 2-2-3-2-INPUT 4-WIDE 2-INPUT 4-WIDE 2-3-3-2-INPUT 4-WIDE 2-3-3-2-INPUT	3.5 ns 6.6 ns 10.5 ns 12.5 ns 43 ns	29 mW 41 mW 23 mW 4.5 mW 1.5 mW	SN74S64 SN74H54 SN7454 SN74LS54 SN74L54
DUAL 2-WIDE 2-INPUT	3.5 ns 6.5 ns 10.5 ns 12.5 ns 43 ns	28 mW 29 mW 14 mW 2.75 mW 1.5 mW	SN74S51 SN74H51 SN7451 SN74LS51 SN74L51

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
4-WIDE 4-2-3-2-INPUT	5.5 ns	36 mW	SN74S65

EXPANDABLE GATES

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN7423
4-WIDE AND-OR GATES	9.9 ns	88 mW	SN74H52
4-WIDE AND-OR-INVERT GATES	6.6 ns 10.5 ns	41 mW 23 mW	SN74H53 SN7453
2-WIDE AND-OR-INVERT GATES	6.8 ns	30 mW	SN74H55
DUAL 2-WIDE AND-OR-INVERT GATES	6.5 ns 10.5 ns	29 mW 14 mW	SN74H50 SN7450

EXPANDERS

DESCRIPTION	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
DUAL 4-INPUT EXPANDERS	4 mW 6 mW	SN7460 SN74H60
TRIPLE 3-INPUT EXPANDERS	13 mW	SN74H61
3-2-2-3-INPUT AND-OR EXPANDERS	25 mW	SN74H62

BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP. POWER PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	48 mA 24mA 12 mA	− 2.4 mA − 1.2 mA − 1.2 mA	7 ns 12 ns 12 ns	28 mW 5.5 mW 5.5 mW	SN7428 SN74LS28
DUAL 4-INPUT POSITIVE-NAND BUFFERS	60 mA 60 mA 48 mA 24 mA 12 mA	− 3 mA − 1.5 mA − 1.2 mA − 1.2 mA − 1.2 mA	4 ns 7.5 ns 10.5 ns 12 ns 12 ns	21 mW 44 mW 26 mW 4.3 mW 4.3 mW	SN74S40 SN74H40 SN7440 SN74LS40

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP. POWER PER GATE	DEVICE TYPES
QUADRUPLE 2-INPUT POSITIVE-NOR LINE DRIVERS	60 mA	− 40 mA	4 ns	22 mW	SN74S140
DUAL 4-INPUT POSITIVE-NAND LINE DRIVERS	48 mA 48 mA	− 42.4 mA − 29 mA	7 ns 7 ns	28 mW 28 mW	SN74128

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP. POWER PER GATE	DEVICE TYPES
HEX BUFFERS/DRIVERS	30 V 30 V 15 V 15 V	40 mA 30 mA 40 mA 30 mA	13 ns 13 ns 13 ns 13 ns	21 mW 21 mW 21 mW 21 mW	SN7407 SN7417
HEX INVERTER BUFFERS/DRIVERS	30 V 30 V 15 V 15 V	40 mA 30 mA 40 mA 30 mA	12.5 ns 12.5 ns 12.5 ns 12.5 ns	26 mW 26 mW 26 mW 26 mW	SN7406 SN7416
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	15 V 5.5 V 5.5 V 5.5 V	16 mA 48 mA 24 mA 12 mA	13.5 ns 12.5 ns 19 ns 19 ns	10 mW 24.4 mW 4.3 mW 4.3 mW	SN7426 SN7438 SN74LS38
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	5.5 V 5.5 V 5.5 V	48 mA 24 mA 12 mA	11 ns 19 ns 19 ns	28 mW 5.45 mW 5.45 mW	SN7433 SN74LS33

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL HYSTERESIS	TYPICAL DELAY TIME	DEVICE TYPES
HEX SCHMITT TRIGGER INVERTERS	0.8 V	15 ns	SN7414
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.55 V 0.8 V	8 ns 15 ns	SN74S132 SN74132
DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.8 V	16.5 ns	SN7413

GATES WITH 3-STATE TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. POWER DISSIPATION PER GATE	DEVICE TYPES
QUADRUPLE BUS BUFFERS	10 ns 10 ns	40 mW 45 mW	SN74125 SN74126
12-INPUT POSITIVE-NAND-GATES	4.5 ns	45 mW	SN74S134

USEFUL INFORMATION AND TIPS

Unused Inputs NAND, AND

A. Should be taken to V_{CC} when V_{CC} is guaranteed $\leqslant$ 5.5V, or, if V_{CC} is ever $>$5.5V (due to transients, etc.) take to V_{CC} via a series current limiting resistor of value not less than 1kΩ. Several inputs may be connected to one resistor provided that the total input current in the logical 1 state does not cause the input voltage to fall below 2.7V.

B. May be taken to the output of a device whose output is permanently at a logical 1. Many devices in System 74 are characterised to ensure extra fan out in the logical 1 state in order to facilitate this procedure.

C. May be tied to a driven input of the same gate as long as the fan out of the driving gate is not exceeded in the logical 1 state.

NOR OR Inputs

A. Unused inputs should be grounded.

B. May be tied to a driven input of the same gate as long as the fan out of the driving gate is not exceeded when its output is in the logical 1 state.

Input Currents

A. Should not be allowed to exceed 0.5mA per gate input when the input is at a voltage $\geqslant$5.5V (breakdown condition). This current should be limited to 5mA per package.

B. Should not exceed −5mA per gate input or 25mA package total when the input is below ground. This current flows through the input clamp diodes.

Rise and Fall Times

Data rise and fall times should be $\leqslant$50ns when measured between 0.5V and 2.7V levels except for devices with Schmitt inputs, where there is no restriction. If this criteria cannot be met then a Schmitt trigger should be used between the data source and gate input.

LINE DRIVING

Gates whose outputs drive transmission lines should be situated close to the board periphery so as to minimise line ground return impedance. Line grounds are returned to the package ground and not the system ground. The output from a gate that is driving lines (sending end) should not be used as the input to other logical elements, unless the input has Schmitt action. 'Local' decoupling should be applied to line driver gates.

TRISTATE GATES

Ensure that system delays give minimal 'skew' between the enable inputs of gates whose outputs are OR'd together.

GATES

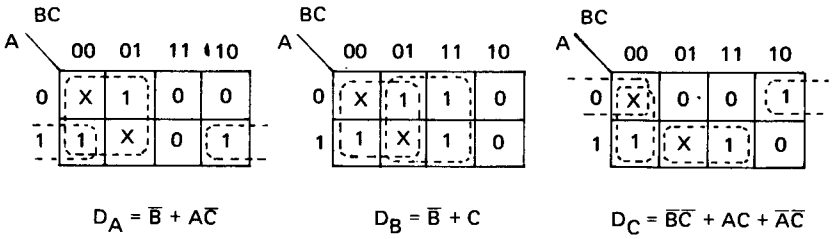
Increased output current in the logical 1 state may be obtained by using a 'pull up' resistor between the output and the V_{CC} supply.

Typical Applications

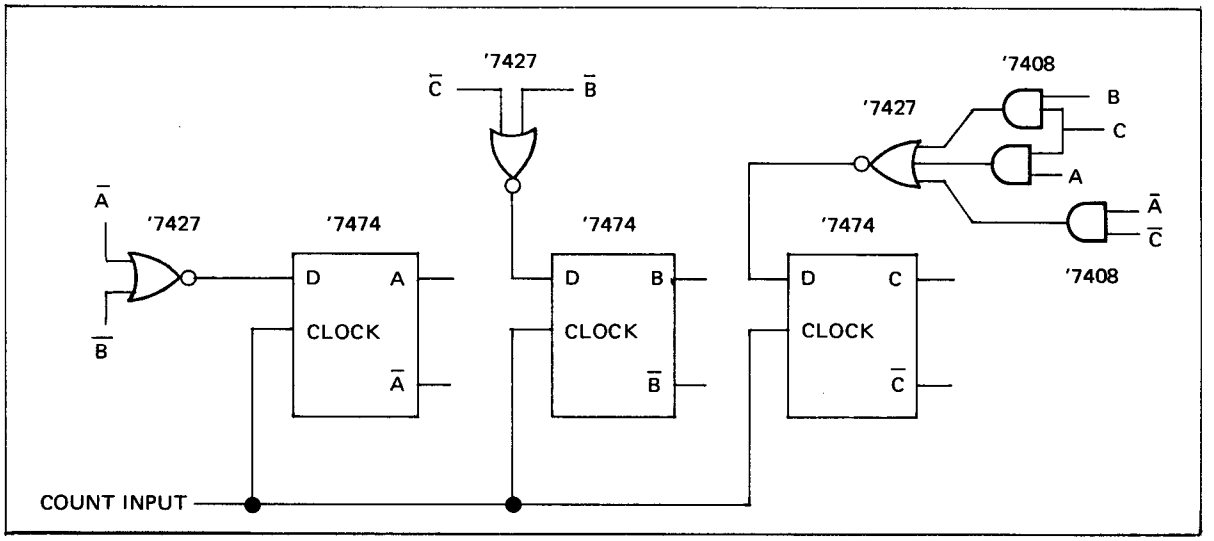
1. Simple 3 stage counter that counts through a predetermined sequence defined by gating functions. Bistables used are D types.

COUNT SEQUENCE

A	B	C
0	1	0
0	0	1
1	1	0
1	0	0
1	1	1
0	1	1
0	1	0

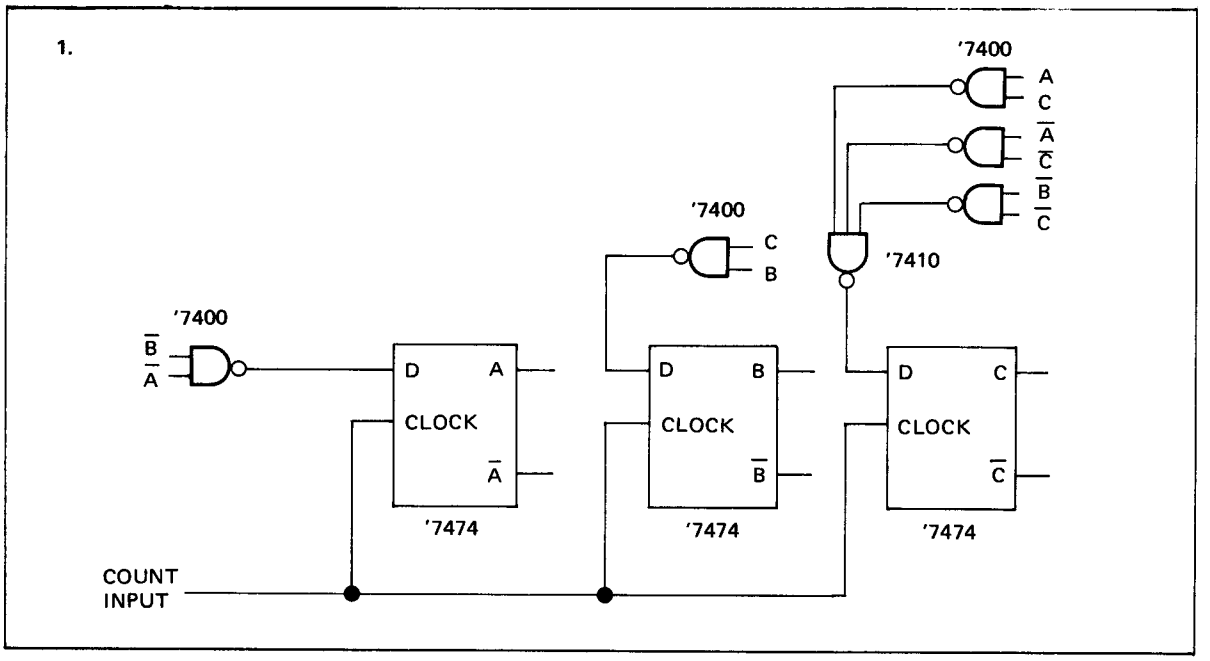


1(a) IMPLEMENTATION



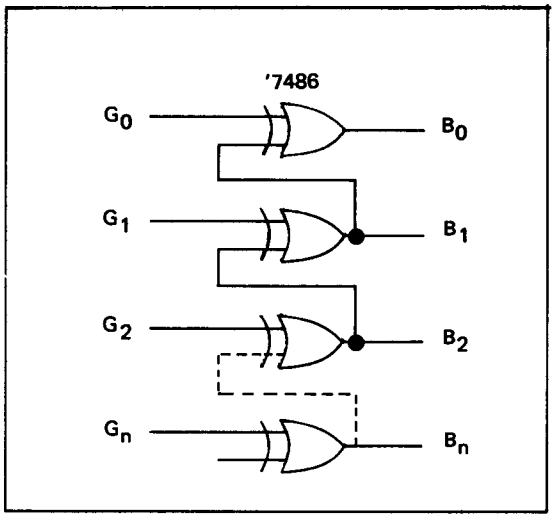
The method shown illustrates the technique of driving the D inputs by the inverse function (NOR) and obtaining the true function (OR) at the $\overline{Q}$ outputs.

1(b) ALTERNATIVELY

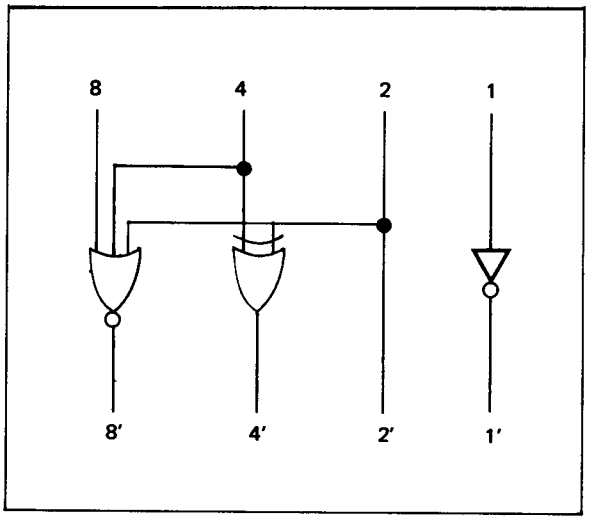


Combinational logic, typical examples

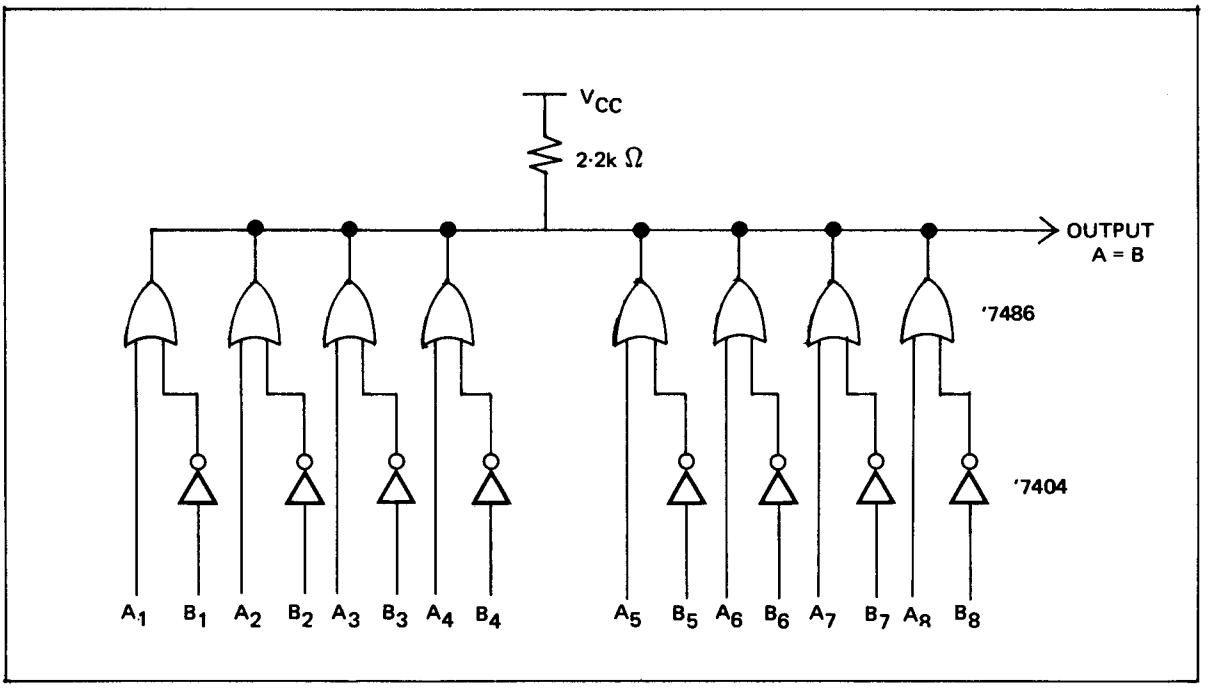
2. Grey code to binary convertor



3. BCD 9's Complementer



4. Open collector exclusive OR used as a binary comparator.



Flip-Flops and Counters

COUNTERS

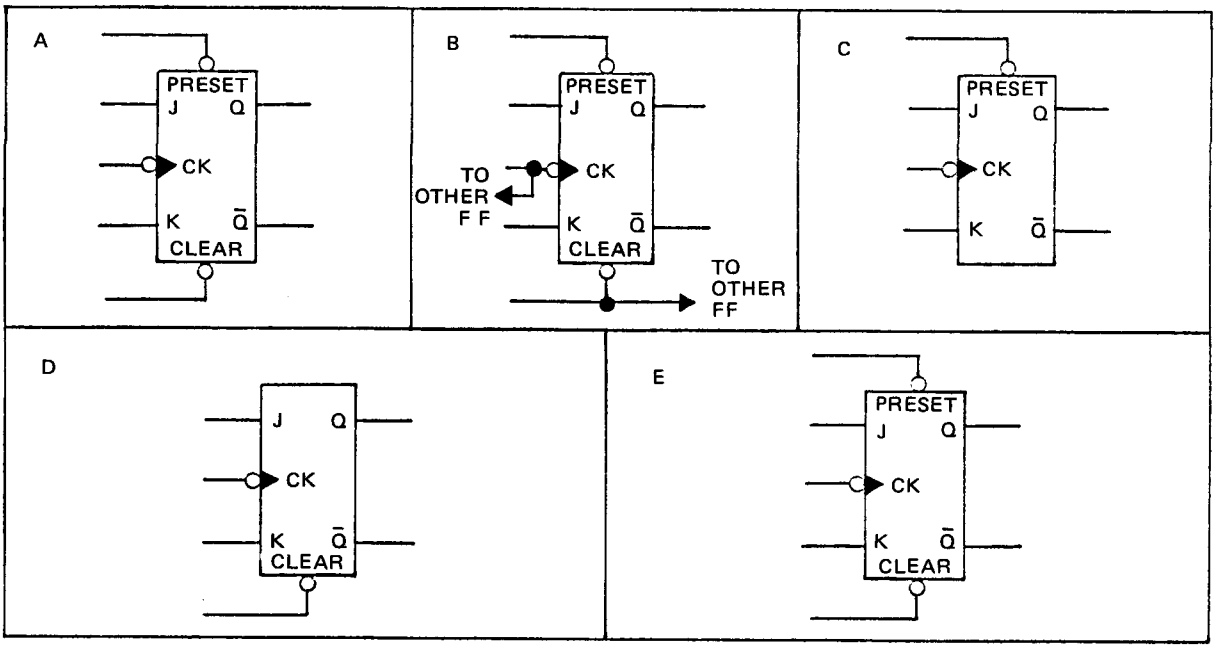
ASYNCHRONOUS COUNTERS (RIPPLE CLOCK)—NEGATIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ.	PARALLEL LOAD	CLEAR	TYP. TOTAL POWER DISSIPATION	DEVICE TYPES	No. OF PINS
DECADE	50 MHz	Yes	Low	240 mW	SN74196	14
	35 MHz	Yes	Low	150 mW	SN74176	14
	32 MHz	Set-to-9	High	160 mW	SN5490A	14
	32 MHz	Set-to-9	High	160 mW	SN74290	14
	30 MHz	Yes	Low	60 mW	SN74LS196	14
	3 MHz	Set-to-9	High	20 mW	SN74L90	14
4-BIT BINARY	50 MHz	Yes	Low	240 mW	SN74197	14
	35 MHz	Yes	Low	150 mW	SN74177	14
	32 MHz	None	High	160 mW	SN7493A	14
	32 MHz	None	High	160 mW	SN74293	14
	30 MHz	Yes	Low	60 mW	SN74LS197	14
	3 MHz	None	High	20 mW	SN74L93	14
DIVIDE-BY-12	32 MHz	None	High	160 mW	SN7492A	14

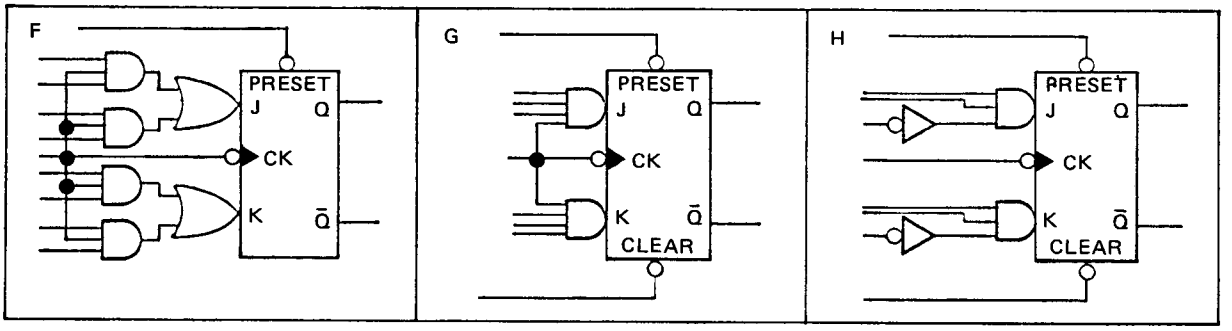
SYNCHRONOUS COUNTERS—POSITIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ.	PARALLEL LOAD	CLEAR	TYP. TOTAL POWER DISSIPATION	DEVICE TYPES	No. OF PINS
DECADE	25 MHz	Sync	Sync-L	305 mW	SN74162	16
	25 MHz	Sync	Async-L	305 mW	SN74160	16
DECADE UP/DOWN	25 MHz	Async	Async-H	85 mW	SN74LS192	16
	25 MHz	Async	Async-H	325 mW	SN74192	16
	20 MHz	Async	None	90 mW	SN74LS190	16
	20 MHz	Async	None	325 mW	SN74190	16
	3 MHz	Async	Async-H	42 mW	SN74L192	16
DECADE RATE MULTIPLIER, $\frac{1}{N_{10}}$	25 MHz	Set-to-9	Async-H	270 mW	SN74167	16
4-BIT BINARY	25 MHz	Sync	Sync-L	305 mW	SN74163	16
	25 MHz	Sync	Async-L	305 mW	SN74161	16
4-BIT BINARY	25 MHz	Async	Async-H	85 mW	SN74LS193	16
	25 MHz	Async	Async-H	325 mW	SN74193	16
	20 MHz	Async	None	90 mW	SN74LS191	16
	20 MHz	Async	None	325 mW	SN74191	16
	3 MHz	Async	Async-H	42 mW	SN74L193	16
6-BIT BINARY RATE MULTIPLIER, $\frac{1}{N_2}$	25 MHz		Async-H	345 mW	SN7497	16

DUAL J-K EDGE-TRIGGERED FLIP-FLOPS



SINGLE J-K EDGE-TRIGGERED FLIP-FLOPS

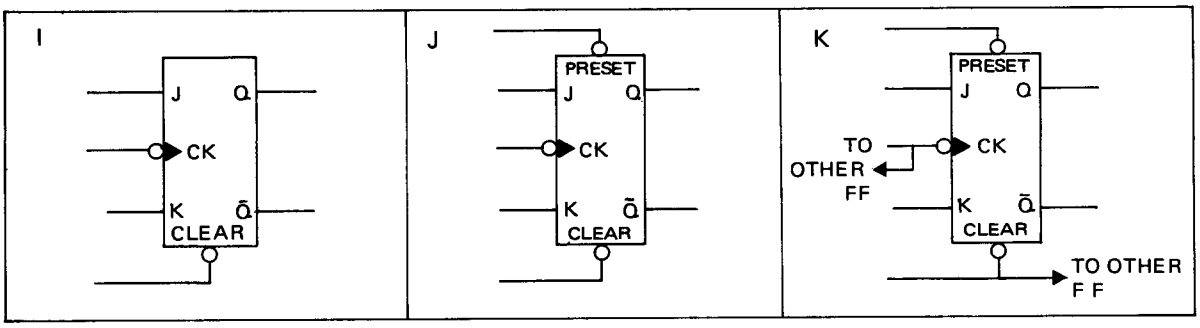


FLIP-FLOP SELECTION GUIDE

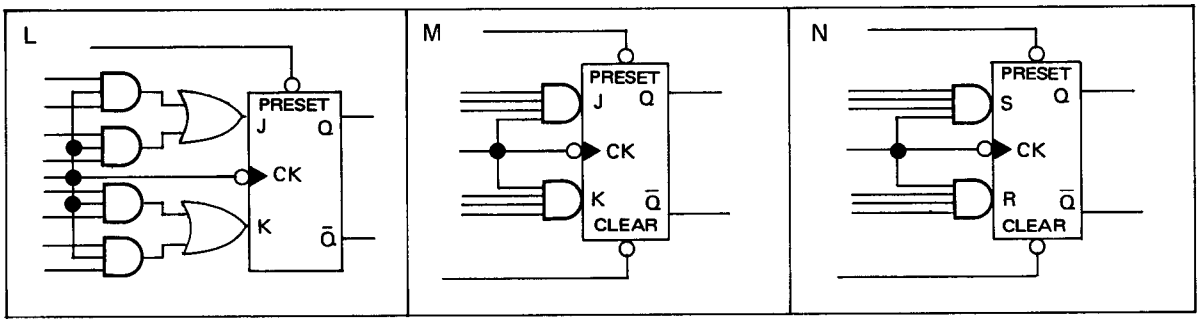
DWG. REV.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPES	No. OF PINS
	$f_{max.}$ (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)		
A	125	75	6↓	0↓	SN74S112	16
	50	100	13↓	0↓	SN74H106	16
	45	10	20↓	0↓	SN74LS76	16
	45	10	20↓	0↓	SN74LS112	16
B	125	75	6↓	0↓	SN74S114	14
	50	100	13↓	0↓	SN74H108	14
	45	10	20↓	0↓	SN74LS78	14
	45	10	20↓	0↓	SN74LS114	14
C	125	75	6↓	0↓	SN74S113	14
	45	10	20↓	0↓	SN74LS113	14
D	50	100	13↓	0↓	SN74H103	14
	45	10	20↓	0↓	SN74LS73	14
E	33	10	20↑	5↑	SN74LS109	14
	33	45	10↑	6↑	SN74109	14
F	50	100	13↓	0↓	SN74H101	14
G	50	100	13↓	0↓	SN74H102	14
H	35	65	20↑	0↑	SN7470	14

↑ ↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

DUAL PULSE-TRIGGERED FLIP-FLOPS



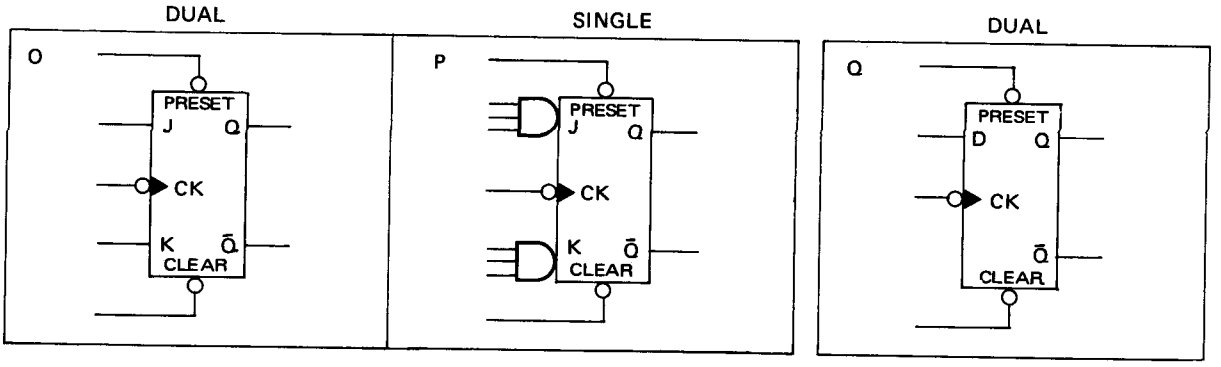
SINGLE PULSE-TRIGGERED FLIP-FLOPS



FLIP-FLOP SELECTION GUIDE

DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPES	No. OF PINS
	$f_{max.}$ (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)		
I	30	80	0↑	0↓	SN74H73	14
	20	50	0↑	0↓	SN7473	14
	20	50	0↑	0↓	SN74107	14
	3	3.8	0↑	0↓	SN74L73	14
J	30	80	0↑	0↓	SN74H76	16
	20	50	0↑	0↓	SN7476	16
K	30	80	0↑	0↓	SN74H78	14
	3	3.8	0↑	0↓	SN74L78	14
L	30	80	0↑	0↓	SN74H71	14
M	30	80	0↑	0↓	SN74H72	14
	20	50	0↑	0↓	SN7472	14
	3	3.8	0↑	0↓	SN74L72	14
N	3	3.8	0↑	0↓	SN74L71	14

J-K FLIP-FLOPS WITH DATA LOCKOUT



FLIP-FLOP SELECTION GUIDE

DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPES	No. OF PINS
	$f_{max.}$ (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)		
O	25	70	0↑	30	SN74111	16
P	25	100	20↑	5↑	SN74110	14
Q	110	75	3↑	2↑	SN74S74	14
	43	75	15↑	5↑	SN74H74	14
	33	10	25↑	5↑	SN74LS74	14
	25	43	20↑	5↑	SN7474	14
	3	4	50↑	0↑	SN74L74	14

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

LATCHES

DESCRIPTION	NO. OF BITS	CLEAR	OUTPUTS	TYPICAL DELAY TIME	TYP. POWER POWER DISSIPATION	DEVICE TYPES	No. OF PINS
D_G (CLOCKED) LATCHES	8	Low	Q	11 ns	250 mW	SN74116	24
		None	Q	15 ns	320 mW	SN74100	24
	4	None	Q.Q	15 ns	160 mW	SN7475	16
		None	Q.Q	30 ns	80 mW	SN74L75	16
S-R Latches (SSI)	4	None	Q	12 ns	90 mW	SN74279	16

S-R LATCHES

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP. TOTAL POWER DISSIPATION	DEVICE TYPES	No. OF PINS
QUADRUPLE S-R LATCHES	12 ns	90 mW	SN74279	16

USER TIPS

1. Unused asynchronous inputs such as clear and load should be taken to defined logic levels as described in the section on gates. Unused inputs should never be left 'floating.'

2. Counters should be treated as though they are edge triggered, requiring <50ns rise and fall times on clock inputs. Many devices have internal clock buffers that require fast edges for correct operation.

3. Transmission lines, capacitive and filament lamp loads, should not be driven directly from counter outputs. Such loads can cause loading rules to be violated resulting in incorrect transfer of data. If such loads are to be driven then a buffering gate should be used.

4. If an asynchronous preset or clear is present at the same time as a clock edge, then it should be maintained for a time at least equal to the minimum preset/clear hold time.

5. When asynchronous feedback is used to reset or load a counter in order to shorten its count cycle, ensure that the minimum preset/load pulse width is greater than that specified for correct operation.

6. Synchronous counters do not overcome the problem of transient outputs being produced by decoding gates. There are generally sufficient differential propagation delays between clock inputs and counter outputs to be detected by a gate.

7. Decoded outputs from counters such as 'ripple carry,' 'max/min,' should not be used as clocks to counters or memory devices unless they are gated to ensure that they are transient free.

Typical Applications

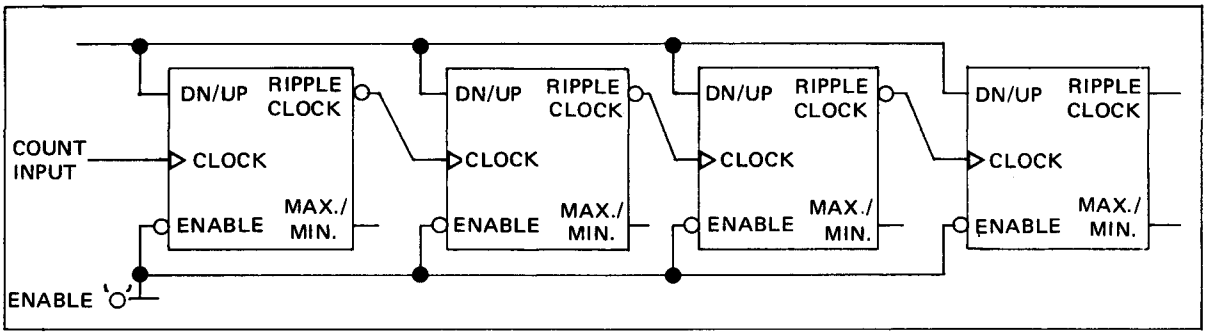
Counters may be cascaded in three ways.

1. Ripple clock, where the changing output of a counter clocks the succeeding stage.
   This mode of operation can be very fast. It allows the user to obtain a good power speed product for the complete counter by using high speed devices at the counter 'front end,' medium in the middle and low speed, low power devices at the end.
   Disadvantages are long settling time compared to count speed, and when parallel loaded with data care has to be taken to ensure that the loaded data does not clock succeeding stages. The count direction of some reversible counters cannot be changed when the clock is in a particular state with this mode of operation.

2. Synchronous, ripple enable.
   In this mode all counters are clocked together (synchronously). Each counter, when it and the preceding stages are full, produces an output which enables the succeeding counter, allowing it to change on the next clock pulse. This mode of operation gives minimal output settling time, but the maximum frequency of operation reduces as further stages are added due to the 'ripple' action of the enable signal.

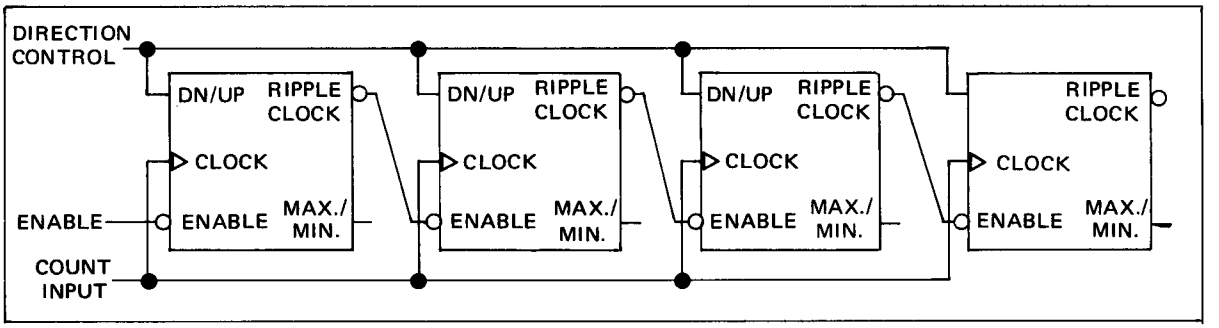
3. Synchronous, parallel look ahead enable.
   Again, all counters are clocked in parallel, but the enable function is generated separately for each stage. This can be achieved with parallel gating or with a carry look ahead package.
   As examples various methods of cascading the SN74190 and SN74160 series of 4 bit counters will be described.

SN74190 Ripple Clock Mode



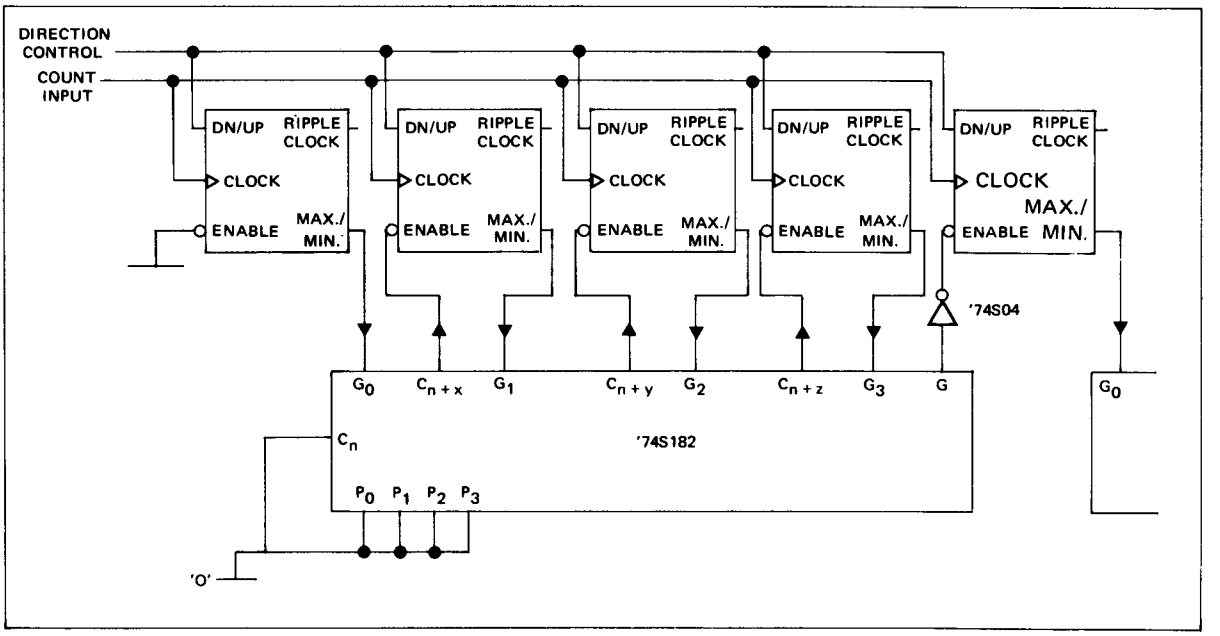
Note: Do not change count direction when clock is low if operated in this mode.
If a particular stage is full or empty a ripple clock to the next stage will be produced.

SN74190 Synchronous clock, ripple enable



The maximum clock frequency is determined by the time taken for the ripple clock-enable to ripple through to the last stage. All outputs change synchronously and the count direction control may be changed independent of the clock line state.

SN74190 Synchronous clock, parallel enable



The carry generate section of the SN74182 provides a convenient means of obtaining the required enable functions with minimal delays.

Up/Down Divide-by-5 Counter

Often a count to a base other than 10 or 16 is required. This means presetting or clearing when a certain number is reached. Fully synchronous counters such as the '162 and '163 make this easy. An up/down counter based on the '190 family requires a little more thought.

Consider a divide by 5 counter with the desired states equivalent to 0, 1, 2, 3 and 4. When counting up and at 4 the output must next go to 0, and when counting down from 0, 4 must be next. Figure 1 shows a possible count sequence and some of the outputs from either a '192 or '193. These devices can be cleared to obtain 0 and loaded to obtain 4. It will be seen that the 0 to 4 change comes at the end of the borrow pulse. It is therefore necessary to use the positive going edge to load the counter. The load (and clear) pulse for the standard '192 and '193 is 20ns minimum. A sufficiently long pulse can be obtained by using the circuit of Figure 2.

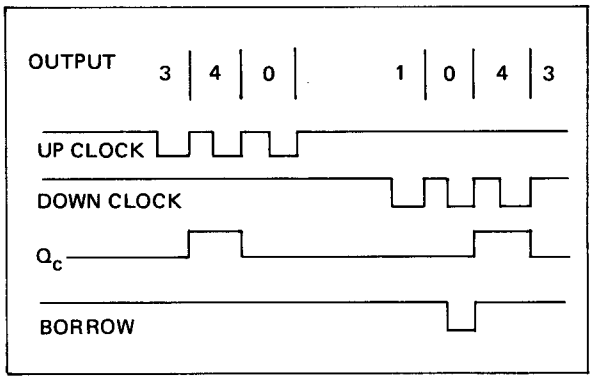


Figure 1

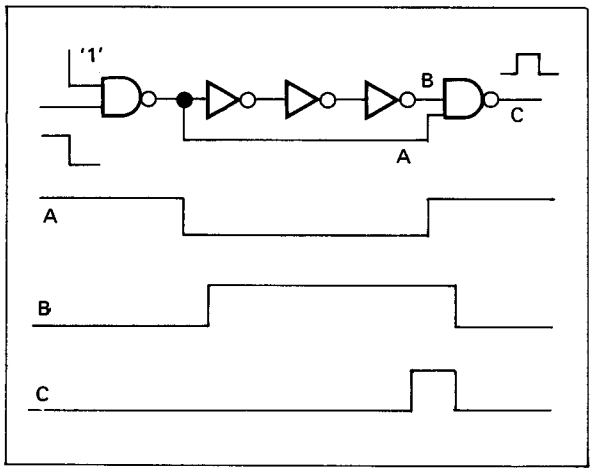


Figure 2

The low power gates have a typical propagation delay of about 30ns. Using three in series will give a sufficient propagation delay to give an ample load pulse.

Gating the up clock pulse with the QC and putting it through such an edge detector will generate a pulse which can be used to clear the counter to 0.

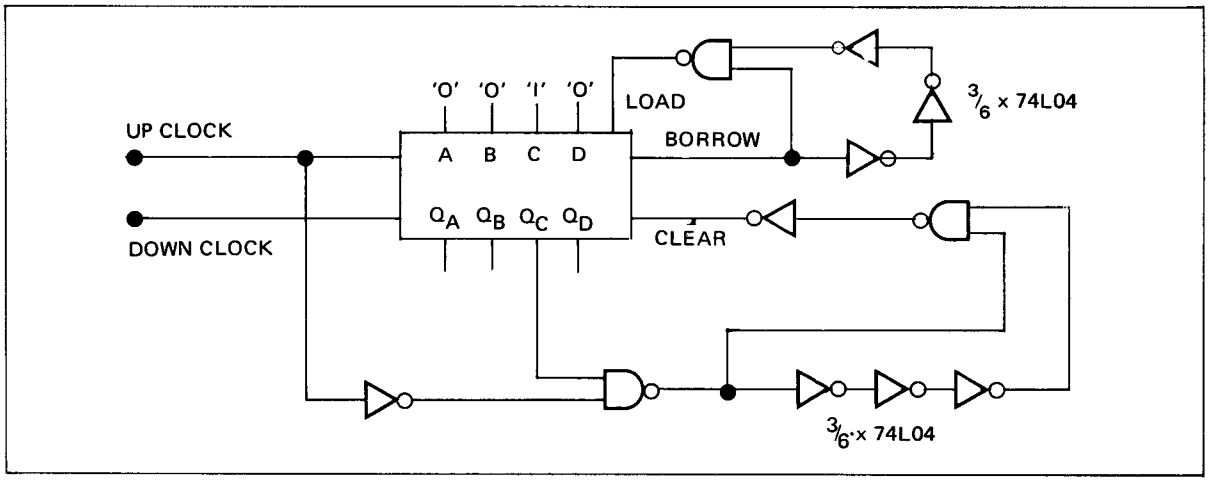


Figure 3.

Dead End Counter

Another thing which is often required is a dead end counter. This is a counter which counts so far but will not go beyond a certain limit. If it is reversible (and one could conceive of an unidirectional version), it will count between two limits. An example might be in a digital servo loop where there ought to be an end stop on the error signal or in trying to increase its value from the maximum count it suddenly steps to the minimum.

Figure 4 shows two possible ways of obtaining a 0 to 9 dead end counter.

Figure 4 (a) inhibits the clock input by using the max. and min. output.

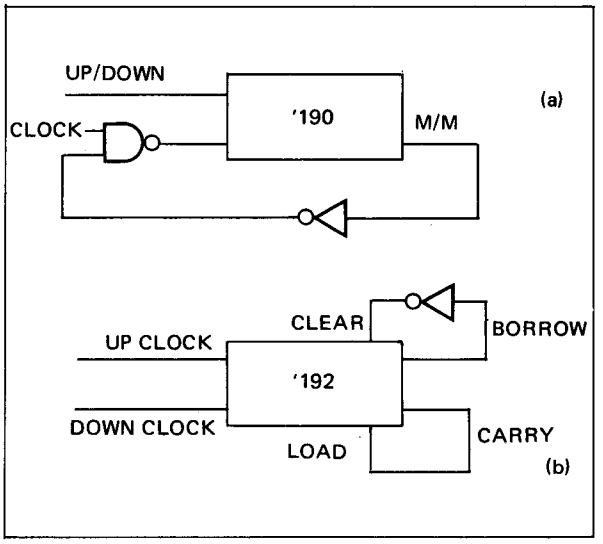


Figure 4

Because this max. and min. output is internally gated with the direction control line changing the Up/Down input will remove the clock inhibit. Figure 4 (b) uses the carry output which is produced when the counter normally overflows from nine to nought to reload nine, and similarly the borrow output to clear back to zero.

Other values of end stops can be chosen. Figure 5 shows an example. The upper limit, which inhibits the Up Clock, is chosen as 1011, i.e. 13.

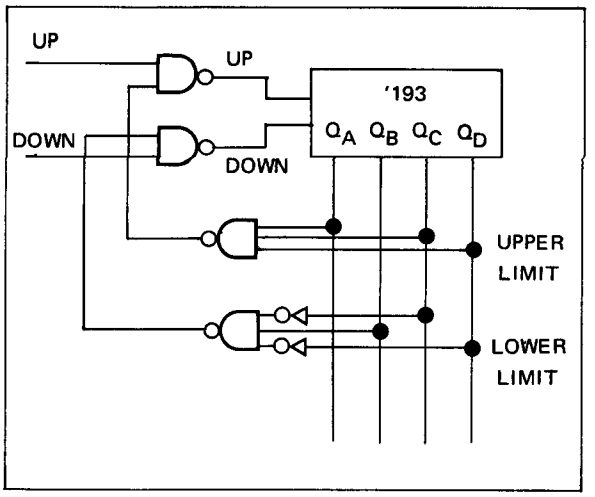
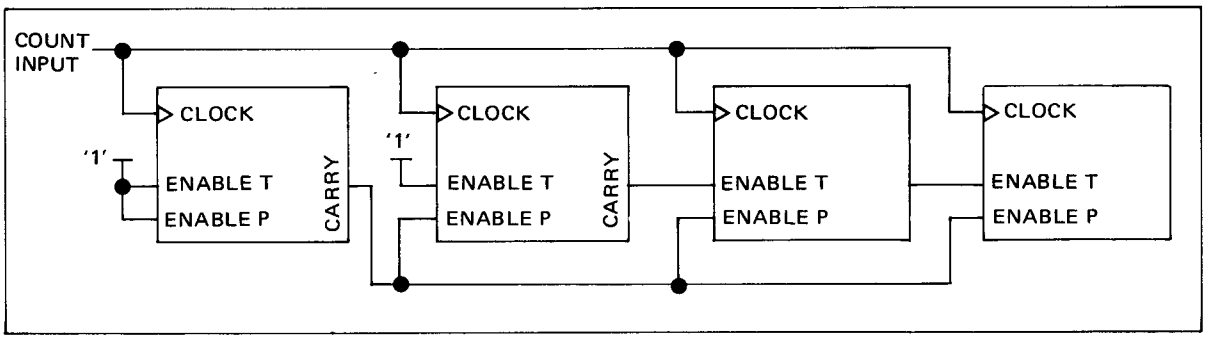


Figure 5.

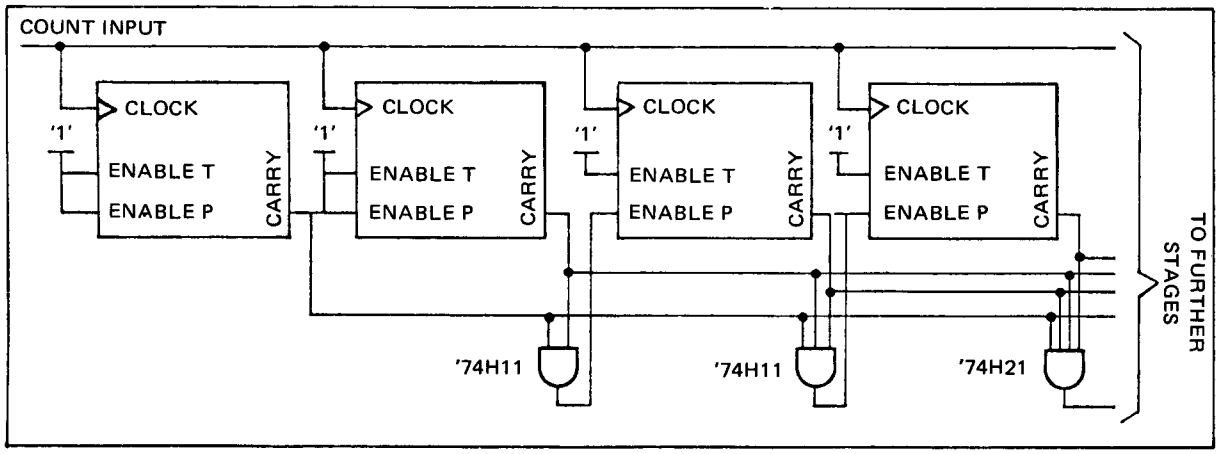
The lower limit is X100, (where X represents a 'don't care' condition) i.e. 2 or 3. The first of these values reached when counting down is 3. Therefore the end stops will be 3 and 13 giving the counter eleven possible states.

The SN74160 series of 'up' counters may be cascaded in ways similar to those shown for the SN74190 series. There is however, one basic difference, that is they have a modified carry look ahead logic incorporated on the chip. A carry from the least significant (fastest cycling) counter is carried forward to *all* of the higher order counters. This carry is then 'ANDed' in each counter with a ripple carry produced from all stages except the first. This method allows 10 or 16 clock periods for the 'ripple enable' signal to run down the counter. The appropriate stages are thereby enabled in parallel by the carry from the least significant counter stage on the next clock pulse.

SN74160 carry look ahead mode

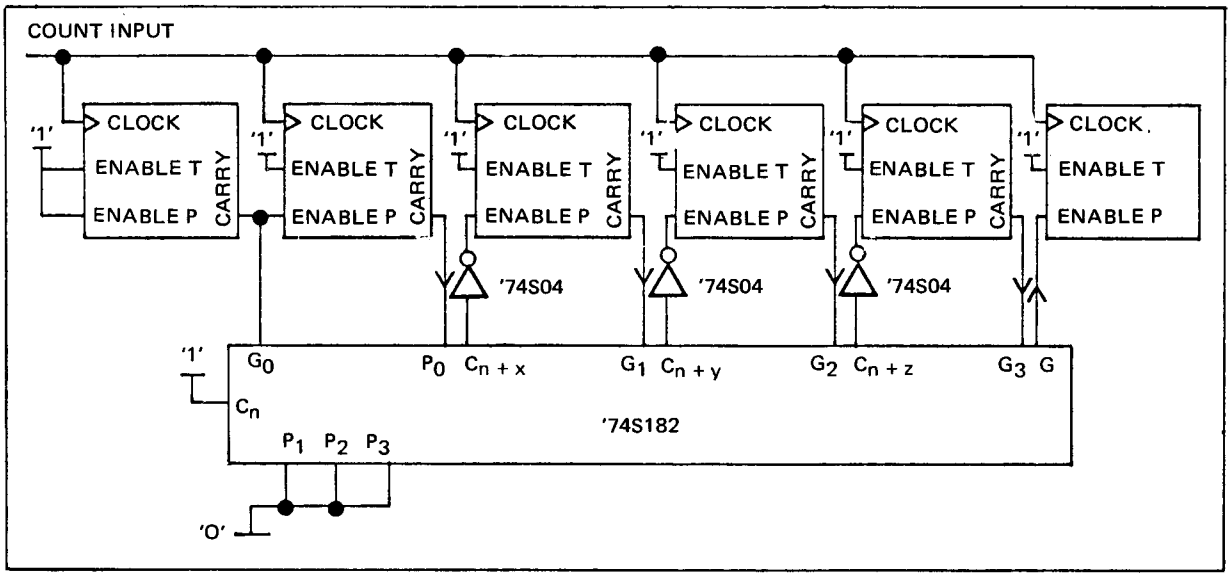


Since the circuit is not a full carry look ahead circuit gate delays can cause sufficient signal skewing to cause problems when the highest operating speed is required. This may be overcome by using enable gating that is fully synchronous as shown.

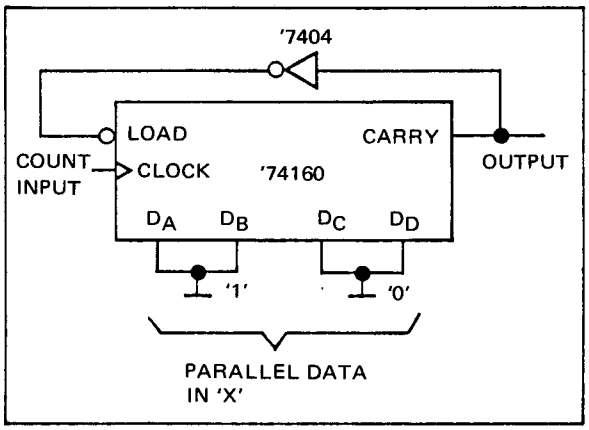


An alternative method of generating the required enable functions would be to use the SN74182 carry look ahead generator. For increased speed Schottky devices may be employed.

SN74162 with carry look ahead SN74S182



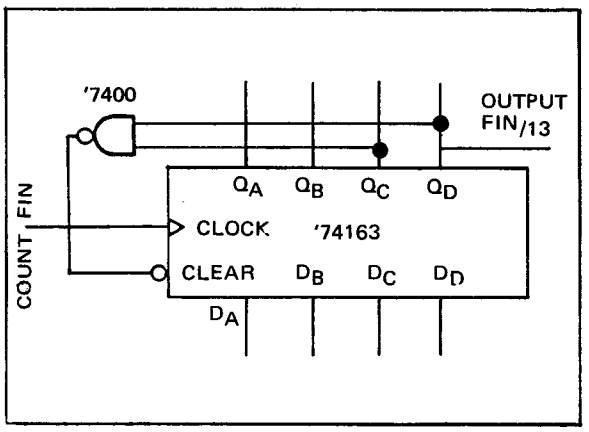
The 160 series of counters may be used to divide to any base using the synchronous parallel load facility. Two methods of changing the counter modulus may be used. The carry output from a modulo N counter may be used to synchronously load a number X into the counter. The counter will then count to a base of (N–X), for example using the SN74160 decade counter to divide by 7, here N = 10 and X = 3.



COUNT SEQUENCE

	D	C	B	A	
→	0	0	1	1	LOAD
	0	1	0	0	
	0	1	0	1	
	0	1	1	0	
	0	1	1	1	
	1	0	0	0	
	1	0	0	1	CARRY PRODUCED
	0	0	1	1	3 LOADED

This method can, of course, be expanded to cover more than one decade. If a sub-multiple of the input clock is required, this may be obtained from the carry output after gating with the clock to remove transients.



The second method is to detect when the counter reaches a number, one less than the base, and then to synchronously clear it to zero. This detection may be carried out using nand gates, comparators or exclusive ORs. The example shown illustrates a modulo 13 binary counter.

COUNT SEQUENCE

A	B	C	D	
0	0	0	0	LOAD
1	0	0	0	
0	1	0	0	
1	1	0	0	
0	1	0	1	
1	1	0	1	
0	0	1	1	ENABLE LOAD
0	0	0	0	

Shift Registers

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	SHIFT FREQ.	SERIAL DATA INPUT	ASYNC CLEAR	MODES S-R	MODES S-L	MODES LOAD	MODES HOLD	TYP TOTAL POWER DISSIPATION	DEVICE TYPES	NO. OF PINS
PARALLEL-IN, PARALLEL-OUT (BIDIRECTIONAL)	8	25 MHz	D	Low	X	X	X	X	360 mW	SN74198	24
	4	70 MHz	D	Low	X	X	X	X	450 mW	SN74S194	16
		25 MHz	D	Low	X	X	X	X	195 mW	SN74194	16
		20 MHz	D	Low	X	X	X	X	60 mW	SN74LS194	16
PARALLEL-IN, PARALLEL-OUT	8	25 MHz	J-K	Low	X		X	X	360 mW	SN74199	24
	5	10 MHz	D	Low	X		X		240 mW	SN7496	16
		5 MHz	D	Low	X		X		120 mW	SN74L96	16
	4	70 MHz	J-K	Low	X		X		375 mW	SN74S195	16
		30 MHz	J-K	Low	X		X		195 mW	SN74195	16
		25 MHz	D	None	X		X		195 mW	SN7495A	14
		25 MHz	D	Low	X		X	X	230 mW	SN74179	16
		25 MHz	D	None	X		X	X	230 mW	SN74178	14
		20 MHz	J-K	Low	X		X		50 mW	SN74LS195	16
		20 MHz	D	None	X		X		50 mW	SN74LS95A	14
		20 MHz	D	None	X		X		62 mW	SN74LS295	14
		3 MHz	J-K	None	X		X		19 mW	SN74L99	16
		3 MHz	D	None	X		X		19 mW	SN74L95	14
SERIAL-IN, PARALLEL-OUT	8	25 MHz	Gated D	Low	X				167 mW	SN74164	14
		12 MHz	Gated D	Low	X				84 mW	SN74L164	14
PARALLEL-IN, SERIAL-OUT	8	25 MHz	D	None	X		X	X	210 mW	SN74165	16
		20 MHz	D	Low	X		X	X	360 mW	SN74166	16
	4	10 MHz	D	High	X		X		175 mW	SN7494	16
SERIAL-IN, SERIAL-OUT	8	10 MHz	Gated D	None	X				175 mW	SN7491A	14
		3 MHz	Gated D	None	X				17.5 mW	SN74L91	14

S R = shift right, S-L = shift left

REGISTER FILES

DESCRIPTION	TYPICAL ADDRESS TIME	TYP READ ENABLE TIME	DATA INPUT RATE	TYP TOTAL POWER DISSIPATION	DEVICE TYPES	NO. OF PINS
EIGHT WORDS OF TWO BITS	33 ns	15 ns	20 MHz	560 mW	SN74172	24
FOUR WORDS OF FOUR BITS	30 ns	15 ns	20 MHz	635 mW	SN74170	16

OTHER REGISTERS

DESCRIPTION	FREQ.	ASYNC CLEAR	TYP TOTAL POWER DISSIPATION	DEVICE TYPES	NO. OF PINS
HEX D-TYPE REGISTERS	75 MHz	Low	450 mW	SN74S174	16
	30 MHz	Low	65 mW	SN74LS174	16
	25 MHz	Low	225 mW	SN74174	16
QUADRUPLE D-TYPE REGISTERS	75 MHz	Low	300 mW	SN74S175	16
	30 MHz	Low	45 mW	SN74LS175	16
	25 MHz	Low	150 mW	SN74175	16
QUADRUPLE MULTIPLEXERS WITH STORAGE	25 MHz	None	195 mW	SN74298	16
	3 MHz	None	25 mW	SN74L98	16
QUADRUPLE BUS-BUFFER REGISTERS	25 MHz	High	250 mW	SN74173	16

USER TIPS

1. Unused inputs such as preset/clear should be taken to defined logic levels and not left 'floating'.
2. Shift register clock inputs should be treated as though they are edge triggered, requiring <50ns rise and fall times.
3. Transmission lines, capacitive and filament lamp loads should not be driven directly from register outputs.
4. If an asynchronous preset or clear is present at the same time as a clock edge, then it should maintain for a time at least equal to the minimum preset/clear hold time.
5. Ensure that there is minimal time skew between data and clock on interconnected registers. This may be caused by logic delays, interconnection lengths, etc. If this cannot be avoided then variable skew JKs should be used.
6. Registers with clock input selection gates should only have the mode control changed when both clock inputs are inactive, i.e. logical 0. If the mode control is changed when one or both clock inputs are high a spurious clock to the register may be produced.
7. Registers whose first stage is a JK master slave should not have J and K input data changed when the internal clock is high. If however the first stage is an RS that has been logically modified by feed back to perform the JK function, this restriction does not apply. e.g. 74S195, 74199.
8. When decoding output states from registers with gates there is usually sufficient data skew to produce false outputs from the gates as data is shifted.
9. Data should be present at the data inputs for a time at least equal to or greater than the data set up time before the clock is applied. The clock edge to which this time is referenced is that which causes output data to change. The only exception to this is the variable skew master slave.

Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	COUNT
1	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	2
0	0	1	0	0	0	0	0	3
0	0	0	1	0	0	0	0	4
0	0	0	0	1	0	0	0	5
0	0	0	0	0	1	0	0	6
0	0	0	0	0	0	1	0	7
0	0	0	0	0	0	0	1	8

Applications

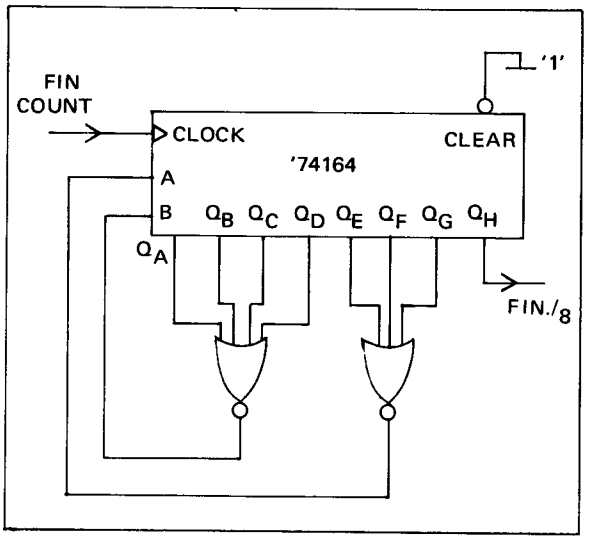
1. Ring Counters

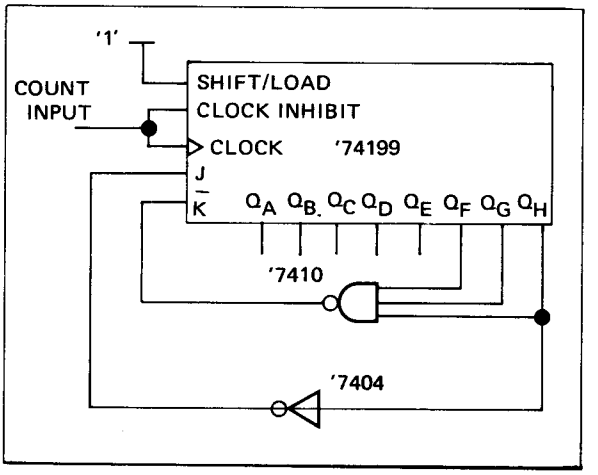
Ring Counters may be used as sequence generators, multiplexers, dividers, etc.

The simple ring counter illustrated is self starting and correcting and will operate at frequencies in excess of 12MHz. The division ratio is N where N is the number of register stages. The principle may be extended to any value of N. The two multi-input gates form with the 2 input AND gate at the register input a 7 input OR gate acting as an AND gate for zeroes. For a value of N the number of gate inputs required is N−1. This counter has the advantages that it is self correcting and the outputs are transient free.

2. Johnson, twisted ring counters

A shift register may be made to divide by 2N by inverting the output and using this as the input to the register. Additional logic must be used to ensure that the correct count sequence is maintained. The examples show 4 and 8 stage counters.

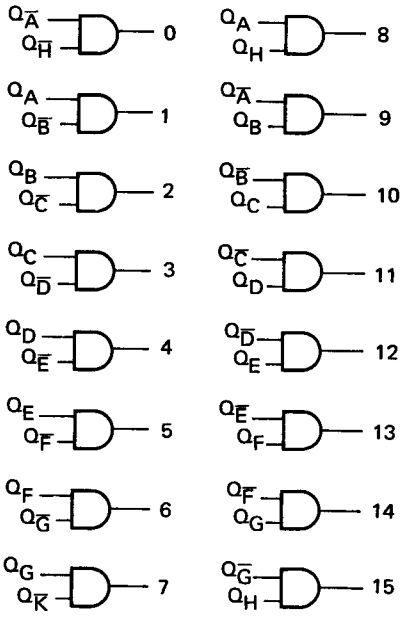




COUNT SEQUENCE

COUNT INPUT	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1
9	0	1	1	1	1	1	1	1
10	0	0	1	1	1	1	1	1
11	0	0	0	1	1	1	1	1
12	0	0	0	0	1	1	1	1
13	0	0	0	0	0	1	1	1
14	0	0	0	0	0	0	1	1
15	0	0	0	0	0	0	0	1

DECODING GATES



An N stage Johnson counter will sequence through 2N gates. They have the advantage that only two input gates are required to decode any state. The count sequence is obtained by inverting the output from the last register stage and using this as the serial input to the first stage. Additional gating is again required to ensure that the counter will always sequence through the correct states and not 'stick' in one of the remaining $(2^8 - 16)$ states. The number of inputs to the nand gate that carries out this correction varies as the number of register stages N varies.

Number of inputs required = next integer above $\frac{N}{3}$, in the example shown N = 8, $\frac{N}{3}$ = 2,67 therefore the nand gate requires 3 inputs.

Decoders and Multiplexers

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL DELAY TIMES			TYP TOTAL POWER DISSIPATION	DEVICE TYPES	No. OF PINS
		DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE			
16-LINE-TO-1-LINE	2-state	11 ns		18ns	200 mW	SN74150	24
8-LINE-TO-1-LINE	3-state	4.5 ns	8 ns	14 ns	275 mW	SN74S251	16
	3-state	17 ns	21 ns	21 ns	250 mW	SN74251	16
	3-state	17 ns	21 ns	21 ns	35 mW	SN74LS251	16
	2-state	4.5 ns	8 ns	9 ns	225 mW	SN74S151	16
	2-state	8 ns	16 ns	22 ns	145 mW	SN74151A	16
	2-state	11 ns	18 ns	27 ns	30 mW	SN74LS151	16
DUAL 4-LINE-TO-1-LINE	3-state		12 ns	16 ns	35 mW	SN74LS253	16
	2-state		6 ns	9.5 ns	225 mW	SN74S153	16
	2-state		14 ns	17 ns	180 mW	SN74153	16
	2-state		14 ns	17 ns	31 mW	SN74LS153	16
	2-state		27 ns	34 ns	90 mW	SN74L153	16
QUADRUPLE 2-LINE-TO-1-LINE WITH STORAGE	2-state		20 ns		195 mW	SN74298	16
	2-state		from clock				
QUADRUPLE 2-LINE-TO-1-LINE	3-state	4 ns		14 ns	280 mW	SN74S258	16
	3-state		5 ns	14 ns	320 mW	SN74S257	16
	2-state	4 ns		7 ns	195 mW	SN74S158	16
	2-state		5 ns	8 ns	250 mW	SN74S157	16
	2-state		9 ns	14 ns	150 mW	SN74157	16
	2-state		18 ns	27 ns	75 mW	SN74L157	16

DECODERS/DEMULTIPLEXERS

	TYPE OF OUTPUT	TYPICAL SELECT TIME	TYPICAL ENABLE TIME	TYP TOTAL POWER DISSIPATION	DEVICE TYPES	No. OF PINS
4-LINE-TO-16-LINE	Totem-Pole	23 ns	19 ns	170 mW	SN74154	24
	Totem-Pole	46 ns	38 ns	85 mW	SN74L154	24
	Open-Collector	24 ns	19 ns	170 mW	SN74159	24
4-LINE-TO-10-LINE BCD-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN7442A	16
	Totem-Pole	34 ns		70 mW	SN74L42	16
4-LINE-TO-10-LINE, EXCESS-3-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN7443A	16
	Totem-Pole	34 ns		70 mW	SN74L43	16
4-LINE-TO-10-LINE EXCESS-3-GRAY-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN7444A	16
	Totem-Pole	34 ns		70 mW	SN74L44	16
3-LINE-TO-8-LINE	Totem-Pole	8 ns	7 ns	225 mW	SN74S138	16
	Totem-Pole	22 ns	21 ns	31 mW	SN74LS138	16
DUAL-2-LINE-TO-4-LINE	Totem-Pole	7.5 ns	6 ns	300 mW	SN74S139	16
	Totem-Pole	22 ns	19 ns	34 mW	SN74LS139	16
	Totem-Pole	18 ns	15 ns	30 mW	SN74LS155	16
	Totem-Pole	21 ns	16 ns	250 mW	SN74155	16
	Open-Collector	23 ns	18 ns	250 mW	SN74156	16

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	DEVICE TYPES	No. OF PINS
BCD-TO-DECIMAL DECODERS/DRIVERS	80 mA 80 mA 7 mA	30 V 15 V 60 V	215 mW 215 mW 80 mW	Invalid Codes Invalid Codes Invalid Codes	SN7445 SN74145 SN74141	16 16 16
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS	40 mA 40 mA 20 mA 20 mA 10 mA	30 V 15 V 30 V 15 V 5.5 V	320 mW 320 mW 133 mW 133 mW 265 mW	Ripple Ripple Ripple Ripple Ripple	SN7446A SN7447A SN74L46 SN74L47 SN7448	16 16 16 16 16

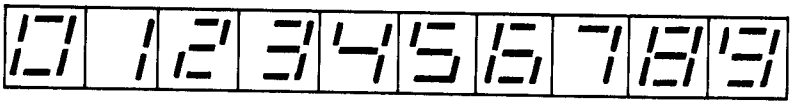
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTER/LATCH

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	DEVICE TYPES	No. OF PINS
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-DECIMAL DECODER/DRIVER	7 mA	55 V	340 mW		SN74142	16
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN SEGMENT DECODER/ LED DRIVER	Constant Current 15 mA	7 V	280 mW	Ripple	SN74143	24
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN-SEGMENT DECODER/ LAMP DRIVER	25 mA	15 V	280 mW	Ripple	SN74144	24

RESULTANT DISPLAYS USING '143, '144



0 1 2 3 4 5 6 7 8 9

User tips

1. Data and decoded outputs are not always transient free due to internal delays in the address decoders. Outputs should always be strobed before driving edge triggered devices.
2. Unused inputs should be taken to defined logic levels. If inputs are left 'open' propagation delays will increase and noise immunity will be degraded.
3. Output lead lengths on Nixie tube decoder/drivers should be minimal in order to reduce transient radiation from the high voltage outputs.
4. With decimal decoders, non BCD input codes may cause more than one output character to appear. Check with data sheet to confirm if this is so.
5. When non valid input codes are used for blanking nixie drivers the anode voltage may be required to be lowered in order to fully blank the display.
6. When using incandescent lamp loads care should be taken to ensure that the peak lamp current does not exceed the device ratings. Most incandescent lamps pass 10–20 times their rated current when cold. Simplest solution is to use VLED displays.

Random Data Selection

Data selectors can select at random one source out of a multitude of information sources, and couple the output of this source through to a single information channel or input. Data inputs can be selected by applying the appropriate binary-coded address to the data-select inputs.

The number of data inputs can be increased by using additional data selectors. A system using two data selectors is shown in Figure 1. When a strobed system is required, the control network of Figure 1a should be used with the network in Figure 1c. Use of the networks of Figures 1b and 1c results in a non-strobed system.

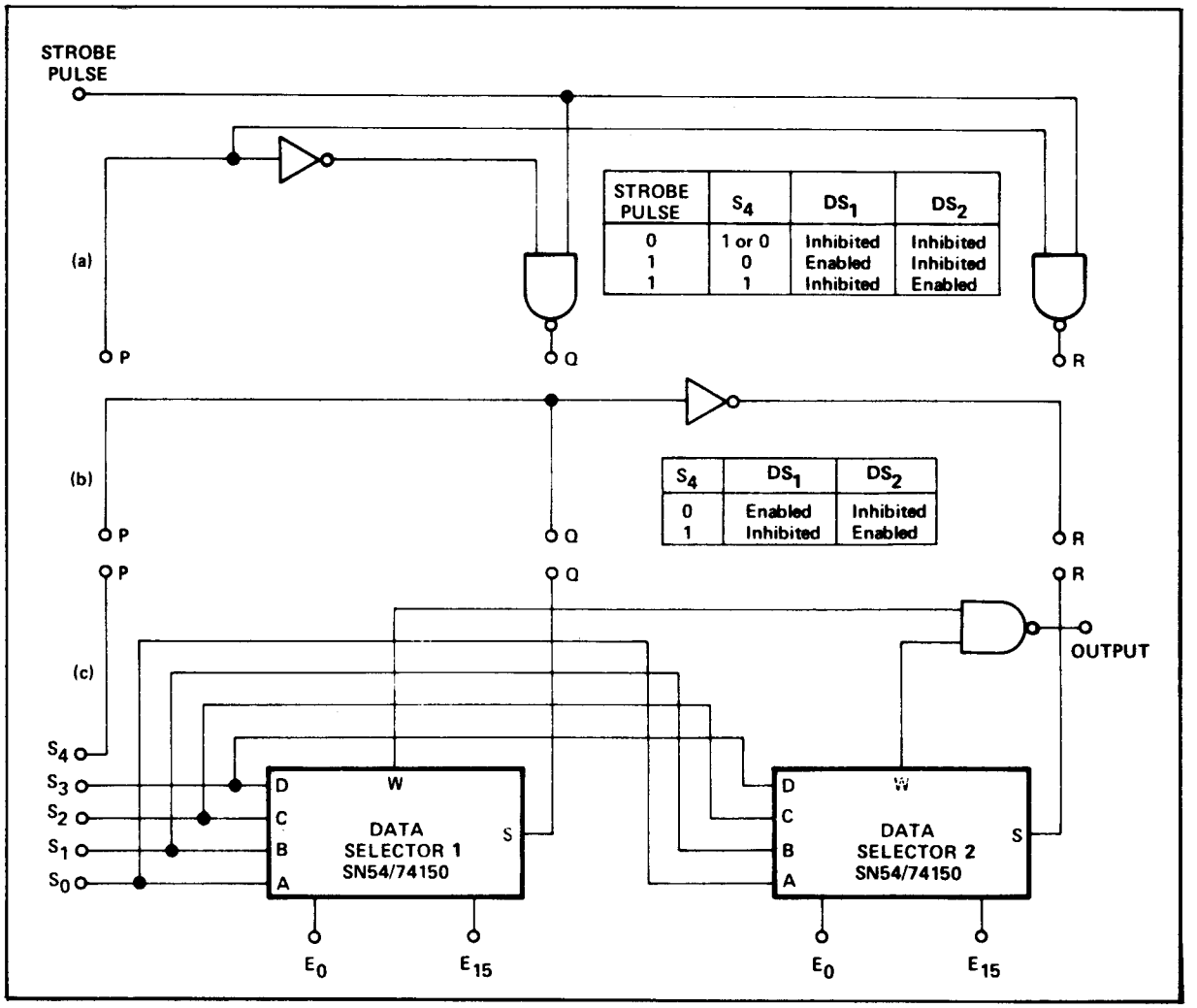


Figure 1. Block Diagram of Data Selectors Being Used to Select 1 out of 32 Information Sources
Control Circuit (b) + Circuit (c) Gives a Non-Strobed System
Control Circuit (a) + Circuit (c) Gives a Strobed System

Sequential Data Selection

Sequential data selection can be performed with data selectors if the data-select address is taken from the outputs of a binary counter (SN7493), as in Figure 2. Operation of such a system resembles that of an electromechanical stepping switch. With each clock pulse, the binary counter switches to the next state, causing the data selector to select in sequence the information sources connected to its data inputs.

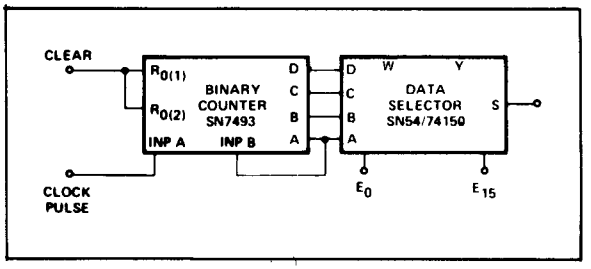


Figure 2. Block Diagram Using a Data Selector to Sequentially Select 1 Out of 16 Information Sources

The number of data-inputs can be expanded by cascading data selectors and using appropriate control networks. A sequential data selection system with 'n' data selectors is shown in figure 3.

In the system shown, two counters are used. Counter 1 supplies the binary coded address to the data selectors. Counter 2 followed by a decoder, to be described later, sequentially enables the data selectors.

Multiplexing to Multiple Lines

In general, multiplexing means transmitting a large number of information units over a smaller number of channels or lines. Consequently, the number of outgoing lines of multiplexing system is not necessarily restricted to one. Multiplexing to multiple lines is necessary for instance when a multitude of words have to be transferred, a whole word at a time. For multiplexing n-bit words, n data selectors are necessary.

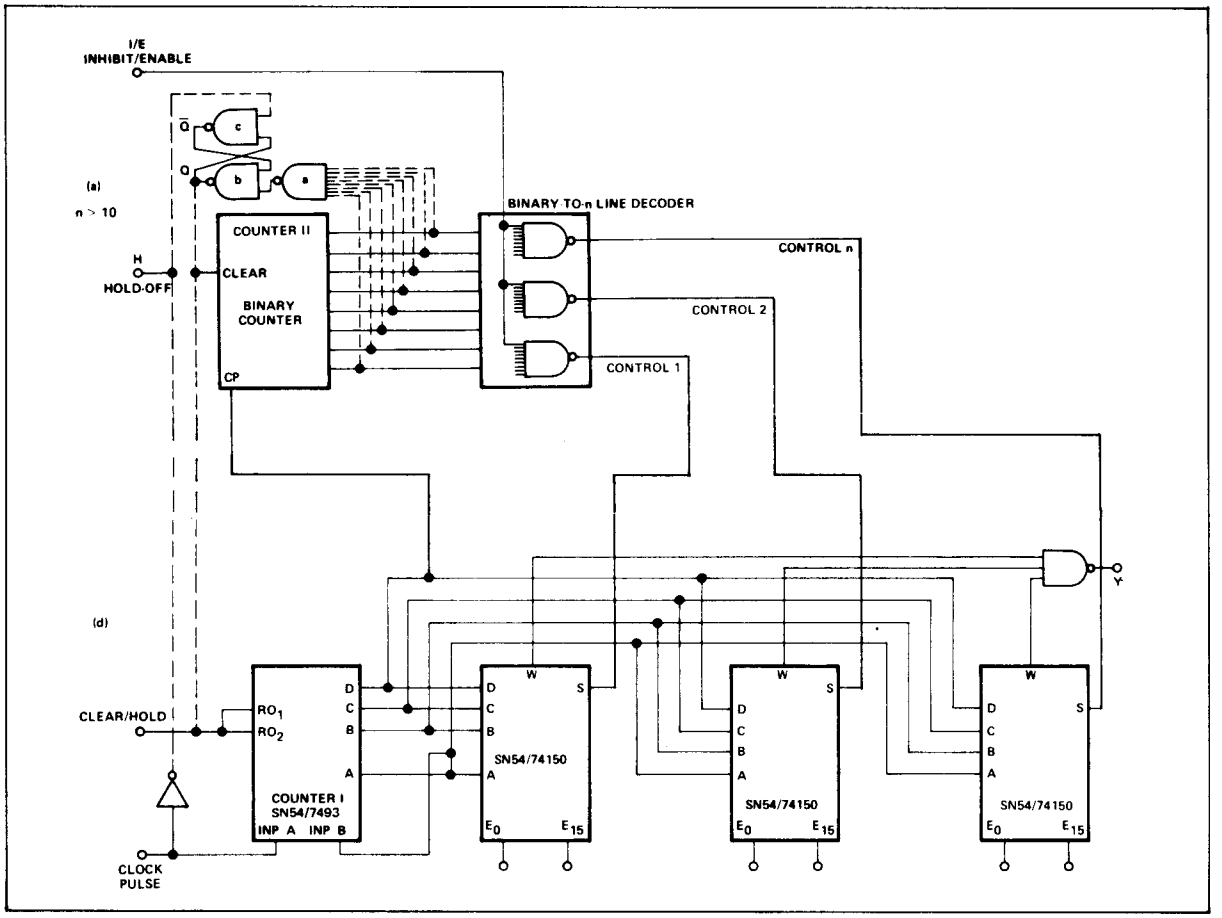


Figure 3. Block Diagram of Data Selectors Being Used for Sequential Selection of 1 out of n X 16 Information Sources

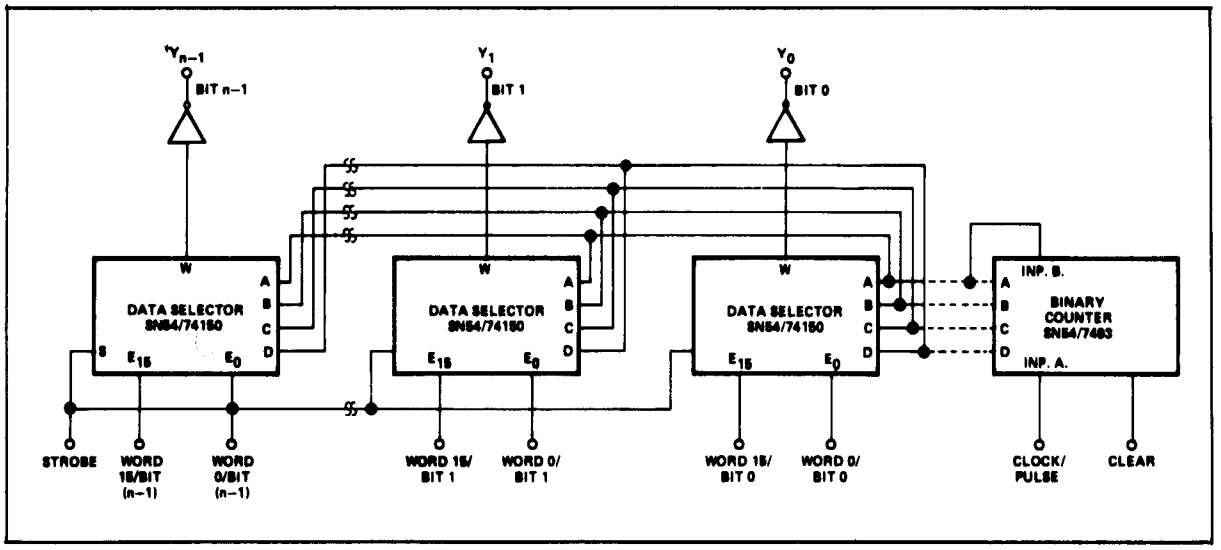


Figure 4. Block Diagram Showing Data Selectors Used to Multiplex Up to 16 Words of n Bits Onto n Parallel Lines

A system for multiplexing up to 16 words of n bits onto n parallel lines is shown in Figure 4. This system can be used either for random word selection, or with a binary counter (SN7493) for sequential word selection.

Data Selectors as Character Generators

Data selectors with a binary counter for sequential selection can be used as character generators. The characters to be generated may be either fixed (wired-in), or manually changeable (switches). Further, they may be controlled and/or determined by a logic system.

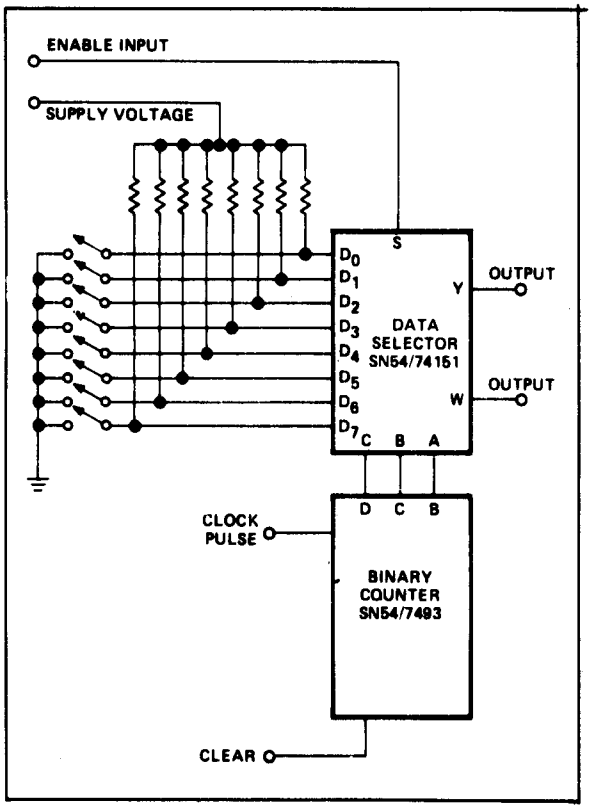


Figure 5. Block Diagram of a 8-Bit Character Generator for Manually Changeable Characters

In Figure 5 a character generator for manually changeable characters using an SN74151 is shown. In fact, every data selector circuit with sequential selection can be used as a character generator. The circuits shown previously can be used as character generators with each character appearing in serial form at the output.

Implementing Logic Functions with Data Selectors

Almost any logic function can be implemented with data selectors. The simplest implementation is obtained when the logic function can be written as a true or an inverted sum of products of its logic variables, because the characteristic logic expression of data selectors is an inverted sum of products.

To implement a given logic function it is necessary to select a data selector which is able to satisfy all (min) terms of the function, directly or through conditioning of the inputs.

For example using the SN74150 and taking the enable input to a logical 0, the logical function obtained at the output is;

$$\overline{F} = \overline{A}\overline{B}\overline{C}\overline{D}E_0 + A\overline{B}\overline{C}\overline{D}E_1 + \overline{A}B\overline{C}\overline{D}E_2 + AB\overline{C}\overline{D}E_3 + \overline{A}\overline{B}C\overline{D}E_4 + A\overline{B}C\overline{D}E_5$$

$$+ \overline{A}BC\overline{D}E_6 + ABC\overline{D}E_7 + \overline{A}\overline{B}\overline{C}DE_8 + A\overline{B}\overline{C}DE_9 + \overline{A}B\overline{C}DE_{10} + AB\overline{C}DE_{11}$$

$$+ \overline{A}\overline{B}CDE_{12} + A\overline{B}CDE_{13} + \overline{A}BCDE_{14} + ABCDE_{15}$$

The logic function to be implemented can be obtained by conditioning the desired minterms, and eliminating unused minterms. A minterm is con-

ditioned by applying the appropriate logic signal to its corresponding data input. Such a conditioning signal can vary from a simple logical "1" to the output signal of a complex gate array of combinational logic. Minterms are eliminated by applying a logical "0" to the appropriate data inputs.

If more minterms than are available are required, they may be created by appropriate conditioning of one or more data inputs and/or using more than one data selector as in Figure 6. Use of n data selectors with m data inputs provide a total of mn minterms.

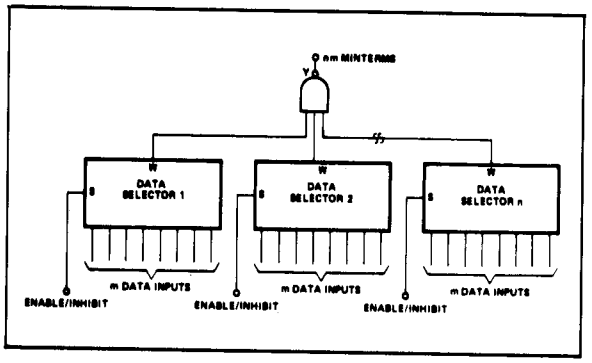


Figure 6. Block Diagram Showing How Minterms Can Be Expanded by Cascading Data Selectors

Decoders

The use of the SN74154 as a 4-line to 16-line decoder is illustrated in Figure 7. Since Enable and Data are at logical "0", the addressed output will be logical "0". This type of circuit is often referred to as a 1-of-16 decoder.

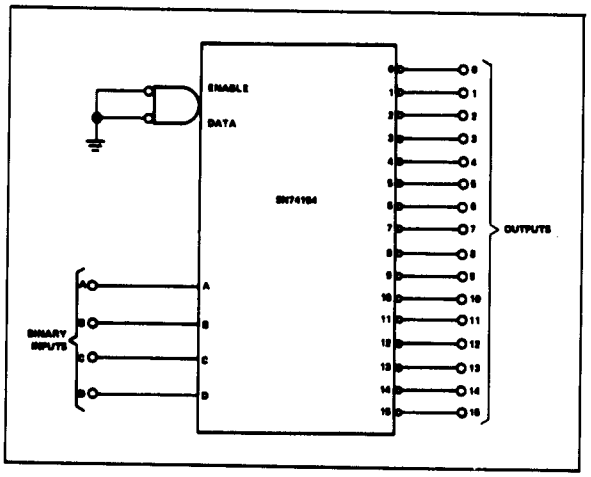


Figure 7. 4-Line-to-16-Line Decoder

Figure 8 illustrates four SN74154 decoders used to decode 6 variables to 1 of 64 lines. Both Enable and Data inputs are used on the four devices to determine which device is activated. Since Enable and Data must be logical "0" to activate a device, proper decoding of the signals at these inputs is necessary to activate only one device at a time.

The above method can be extended to any number of variables with additional SN74154 devices. For instance an 8-line to 256-line (1-of-256) decoder can be constructed with seventeen SN74154 devices. As shown in Figure 8 one SN74154 decoder controls the Data inputs of sixteen others. By controlling the Enable line of device-16, all 256 outputs can be disabled simultaneously.

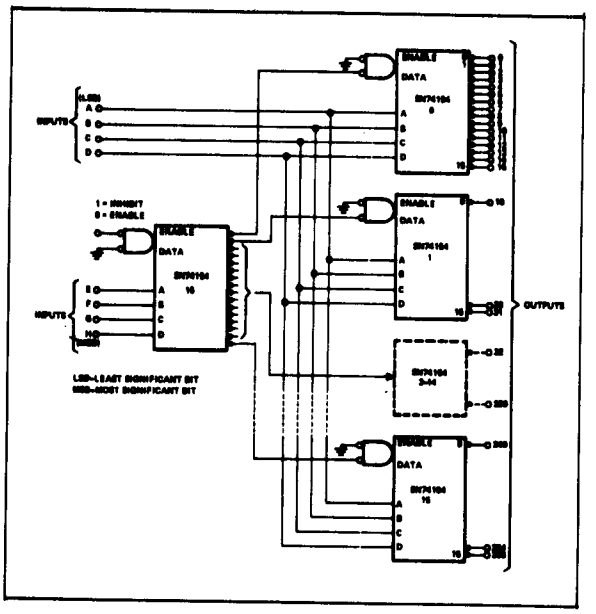


Figure 8. 8-Line-to-Line Decoder with Inhibit Capability

Minterm Generator

When operated as a decoder, the SN74154 can function as low active-output minterm generator producing 16 possible minterms from four variables. The desired minterms can be summed by a positive NAND (negative NOR) gate as illustrated for functions F_1, F_2, F_3, F_4, and F_6 in Figure 9.

Although limited to 10 outputs, the SN7442 4-line to 10-line decoder can be used in decoding applications similar to the SN74154 4-line to 16-line decoder. By use of NOR gates, an ANDing of input variables can be obtained from the outputs of the decoders as shown for functions F_7, F_9, F_{11}, and F_{12}. Since H and I can be any variable, the outputs of other decoders can be used. Therefore, the number of variables ANDed together could far exceed the 9 variables listed for F_{12}.

Code Decoders

Several special purpose 4-line to 10-line MSI decoders are available in the SN74 series. An SN7442 BCD-to-Decimal decoder is used for 8421 decoding. An SN7443 Excess 3-to-Decimal decoder decodes Excess-3 inputs directly. It also can decode the 2421 code if the D input is inverted and the outputs

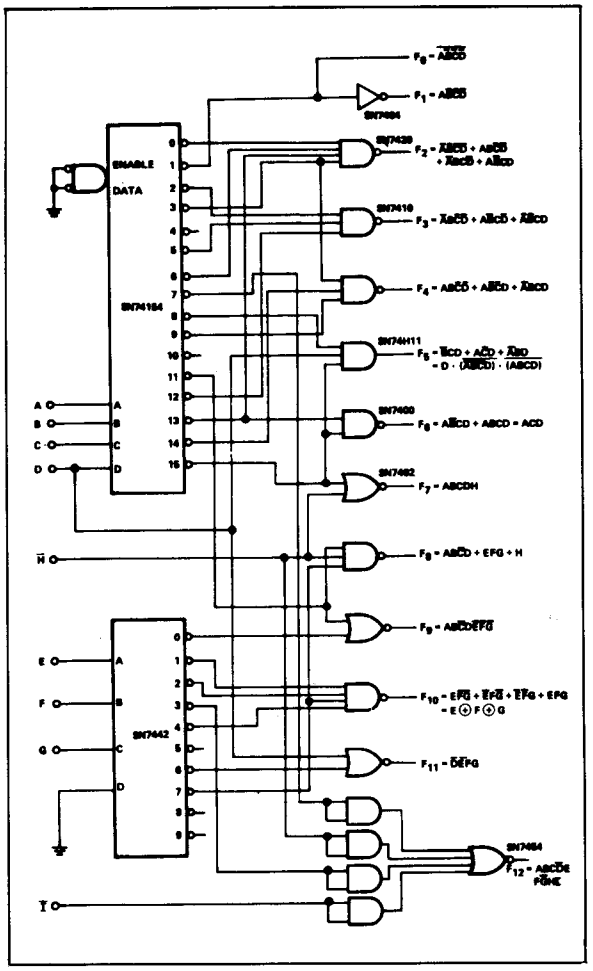


Figure 9. Minterm Generator

rearranged. Excess-3 Gray inputs are decoded by an SN7444 Excess-3 Gray-to-Decimal decoder.

Each special-purpose decoder above accepts only one specific four-bit code. The SN74154 with strobe capability can decode any four-bit code if the appropriate outputs are selected in the desired sequence. For example, Figure 10(a) illustrates the output selection sequence necessary to completely decode the four-bit Gray code. Figure 10(b) shows an output selection matrix by which the SN74154 can decode each of the four-bit decimal codes described above.

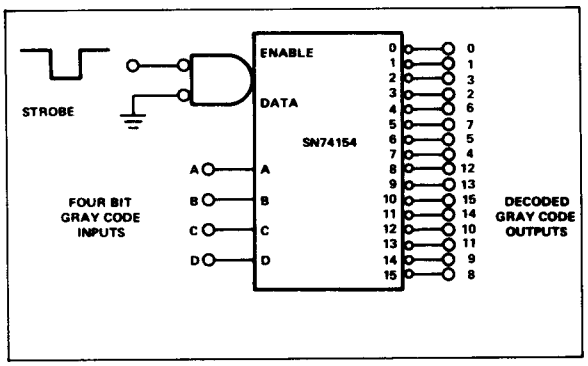


Fig. 10a) Four-Bit Gray Code Decoder

Decimal Digit	SN74154 Output Selection			
	8421	Excess 3	2421	Excess 3 Gray
0	0	3	0	2
1	1	4	1	6
2	2	5	2	7
3	3	6	3	5
4	4	7	4	4
5	5	8	11	12
6	6	9	12	13
7	7	10	13	15
8	8	11	14	14
9	9	12	15	10

Fig. 10b) Output Selection for Decoding Four-Bit Decimal Codes

Figure 10. Using an SN54/74154 To Decode Any Four-Bit Codes by Selecting Appropriate Outputs

Demultiplexer

A typical application of the SN74154 used as a demultiplexer is illustrated in Figure 11. Parallel input data is converted to serial form by an SN74150 16-line to 1-line multiplexer. This serial information is then transmitted to the Data input of an SN74154. By operating the address inputs of the SN74150 and SN74154 synchronously, parallel information is transferred bit-by-bit from the parallel inputs of the SN74150 to the parallel outputs of the SN74154. Latches may then be used to store this data in parallel form.

Multiple bits of data may be transmitted from one parallel input of the SN74150 to the corresponding parallel output of the SN74154. When the system illustrated in Figure 11 is used in this manner, parallel storage latches at the output of the SN75154 are not necessary. Since the SN74150 inverts information, an inverter has been used at its output to re-invert the serial output data. No inversion occurs at the SN74154.

Often the digital transmission system illustrated in Figure 11 is entirely adequate. However, transmission of error-free data over long lines in a noisy environment may require special transmission-line drivers and receivers and careful selection of a suitable transmission line. If necessary, the SN55107 series of Line Drivers and Line Receivers should be used to interface between transmission lines and TTL devices.

Priority Encoders

A priority encoder is basically an N line to binary encoder except that the binary output code always corresponds to the highest order input. For example if inputs 5 and 9 are present then the encoder output code would be binary 9. Priority encoders may be used as conventional encoders if the priority function is not required. As an example the SN74147 is shown as a 10 line to binary keyboard encoder in figure 12.

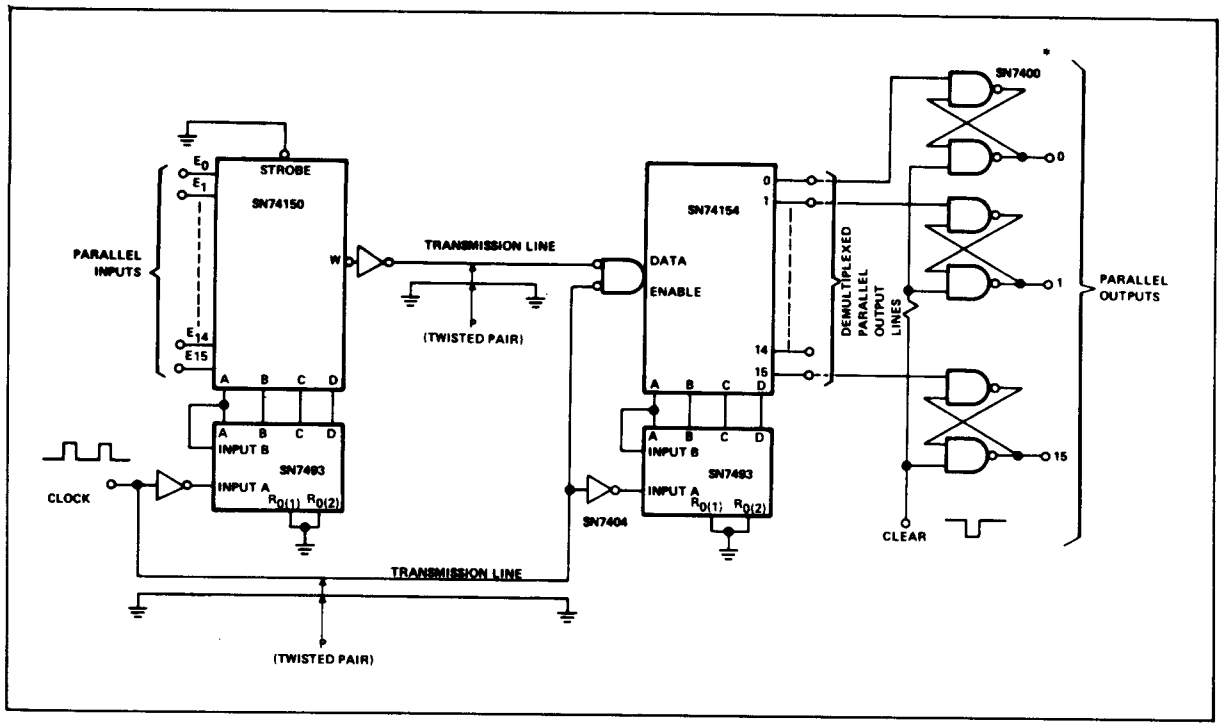


Figure 11. The 16 Line Parallel-To-Serial and Serial-To-Parallel Data Transmission System

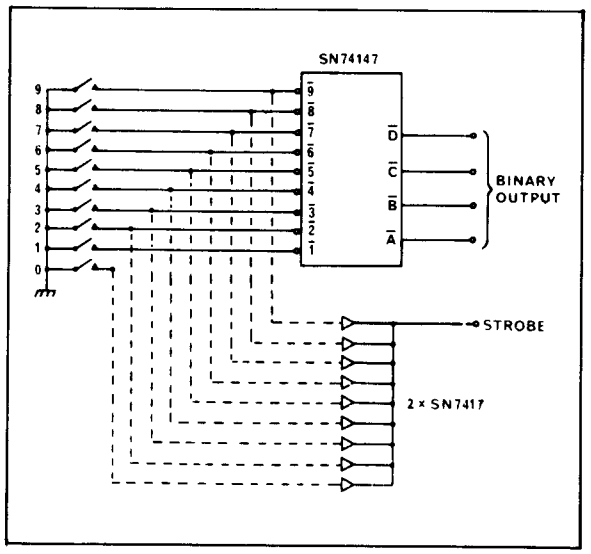


Figure 12. SN74147 as a 10-Line Keyboard Encoder

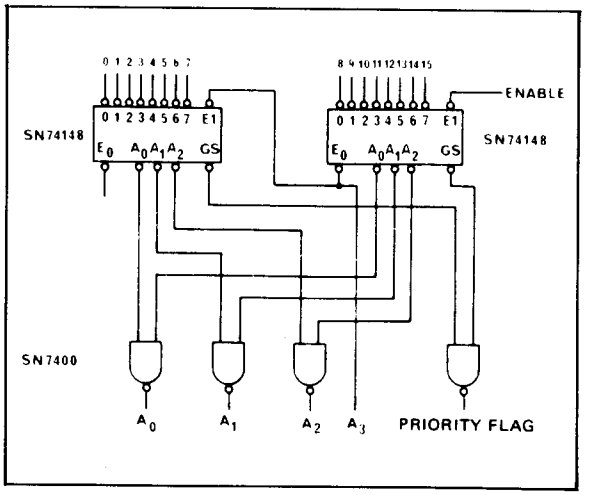


Figure 13. Cascading SN74148 8-Line Priority Encoders

The implied decimal zero position requires no specific input to the encoder since a zero is encoded when all nine input data lines are at a logical 1. The SN74148 8-line priority encoder is provided with an enable input and output together with a group strobe. The strobe indicates if any of the 8 inputs are present and is used when cascading encoders as shown in figure 13.

The 2 input nand gates operate as OR gates for zeros, ORing the outputs of the two encoders.

An application where the priority function is used is shown in figure 14, an 8-bit digital to analogue converter.

The principle on which this circuit operates is to select the most significant binary input for half the cycle time, the next least significant for quarter the cycle time and the next for one-eighth the cycle time etc. The binary inputs to be converted are selected and multiplexed to a single line by an SN74151A. 8

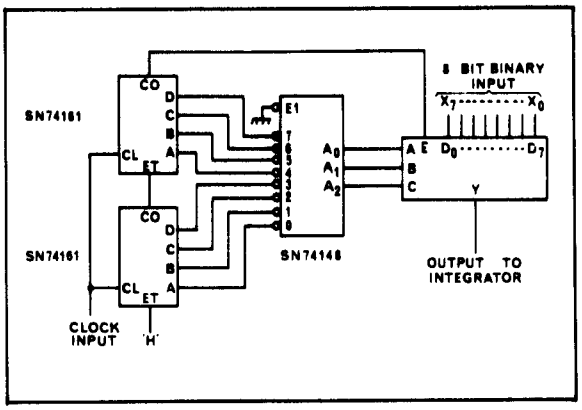


Figure 14. 8 Bit D-A Converter

to 1 line multiplexer. The select inputs are driven by the output of an 8-line priority encoder. The inputs to the priority encoder are obtained from a continuously cycling 8-bit counter. Since the 7's input is connected to the most significant stage of the counter and the 0's input to the least, the output from the priority encoder would be binary 7 for half, binary 6 for quarter, binary 5 for one eighth etc of the counter cycle time.

The output of the SN74151A is therefore a pulse duration modulated signal whose mean value is proportional to the 8-bit binary input. In order to recover the analogue signal the output is fed through a low pass filter.

Arithmetic Devices

ADDERS

DESCRIPTION	TYPICAL CARRY TIME	TYPICAL ADD TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE 0° C to 70° C
SINGLE 1-BIT GATED FULL ADDERS	10.5 ns	52 ns	105 mW	SN7480
SINGLE 2-BIT FULL ADDERS	14.5 ns	25 ns	87 mW	SN7482
SINGLE 4-BIT FULL ADDERS	10 ns 10 ns 50 ns	16 ns 16 ns 33 ns	76 mW 76 mW 19 mW	SN7483A SN74283 SN74LS83
DUAL 1-BIT CARRY-SAVE FULL ADDERS	11 ns	11 ns	110 mW	SN74H183
4-BIT ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS	7 ns 12.5 ns 16 ns	11 ns 24 ns 24 ns	600 mW 455 mW 102 mW	SN74S181 SN74181 SN74LS181
LOOK-AHEAD CARRY GENERATORS	7 ns 13 ns		260 mW 180 mW	SN74S182 SN74182

MULTIPLIERS

DESCRIPTION	TEMPERATURE RANGE 0° C to 70° C
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS (8-BIT PRODUCT IN 40 ns TYPICAL)	SN74284, SN74285
25-MHz 6-BIT-BINARY RATE MULTIPLIERS	SN7497
25-MHz DECADE RATE MULTIPLIERS	SN74167

COMPARATORS

DESCRIPTION	TYPICAL COMPARE TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE 0° C to 70° C
4-BIT MAGNITUDE COMPARATORS	11.5 ns 21 ns 82 ns	365 mW 275 mW 20 mW	SN74S85 SN7485 SN74L85

PARITY GENERATORS/CHECKERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE 0° C to 70° C
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	13 ns	335 mW	SN74S280
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	35 ns	170 mW	SN74180

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE 0° C to 70° C
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH TOTEM-POLE OUTPUTS	7 ns 10 ns 14 ns 55 ns	250 mW 30 mW 150 mW 15 mW	SN74S86 SN74LS86 SN7486 SN74L86
QUADRUPLE 2-INPUT EXCLUSIVE-OR-GATES WITH OPEN-COLLECTOR OUTPUTS	18 ns 27 ns	30 mW 150 mW	SN74LS136 SN74136
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES	18 ns	40 mW	SN74LS266
QUADRUPLE EXCLUSIVE OR/NOR GATES	8 ns	325 mW	SN74S135
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT	14 ns	270 mW	SN74H87

CODE CONVERTERS

DESCRIPTION	TYPICAL DELAY TIME PER PACKAGE LEVEL	TYPICAL TOTAL POWER DISSIPATION	TEMPERATURE RANGE 0° C to 70° C
6-LINE-BCD TO 6-LINE BINARY, OR 4-LINE TO 4-LINE BCD 9's/BCD 10's CONVERTERS	25 ns	280 mW	SN74184
6-BIT-BINARY TO 6-BIT-BCD CONVERTERS	25 ns	280 mW	SN74185A

ARITHMETIC DEVICES

User Tips

1. For correct operation of magnitude comparitors, logic levels on cascade inputs of first stage should be, (A = B) = 1, (A<B) = 0, (A>B) = 0.
2. Many arithmetic devices such as adders, ALUs, exclusive ORs, may be used with negative or positive logic notations. For example, the ALU data sheet specifies negative and positive logic interpretation of the ALU functions.
3. The outputs of a device that have been forced to a logical '1' or '0' by control inputs, may produce transients on these outputs when the input data (operands) are changed. e.g. SN74S181.
4. Carry outputs from adders should be strobed if they are required to clock storage devices. This also applies to ALUs and parity generator outputs.
5. Many ROM 'look up tables' have open collector outputs to allow expansion. Pull up resistors must be used to ensure correct operation. If maximum speed is required the data sheet values (generally 330Ω) should be used, otherwise a value of 39 kΩ will give minimal power dissipation.
6. Combinational logic trees such as 'Wallace' adders need careful choice of device type in order to achieve the best possible speed/power ratio.
7. 'Carry Look Ahead' generators may be used to generate high speed carry enable functions for synchronous counters such as the SN74LS160. This is shown in the section on counters.
8. Unused inputs on adders should be taken to a logical '0' if positive logic convention is used or a '1' if negative convention is used.

ARITHMETIC DEVICES

One of the simplest, but versatile, arithmetic functions is the 'Exclusive OR'. It will perform half adder, parity generation and checking, comparison and code conversion functions. The Exclusive OR of two variables is true if one OR other of the inputs is true but not both, i.e. it is exclusive of both.

The simplest application is as a controlled inverter. The truth table for the SN7486 quad 2 input exclusive OR is shown in figure '1'.

A	B	Y=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

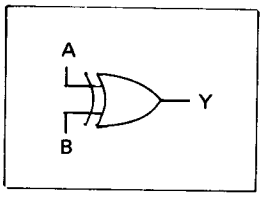


Figure 1.

If the A input is considered to be a control and B the data, then when the control is at a logical 0 the data appears at output Y unchanged. If A is at a logical 1 then the data appears inverted at the output. A four bit controlled 1's complementer (used for subtraction in conjunction with an adder) using the SN74LS86 is shown in figure 2.

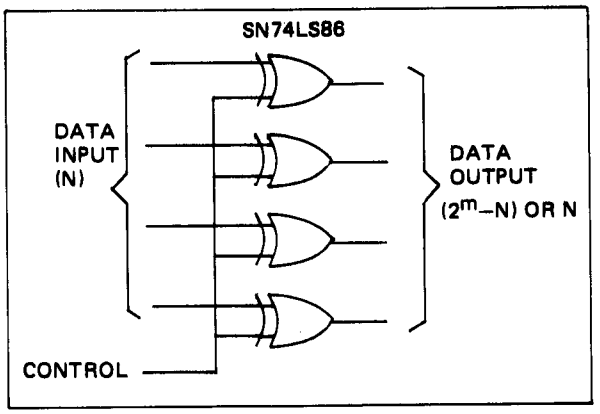


Figure 2.

Further logic may be added to the basic circuit of figure 2 to produce a controllable 'true, zero, complement element'. Such a device is the SN74H87.

Figures 3a and 3b show how the exclusive OR may be used for comparison of two binary words A and B.

Figure 3b requires one of the numbers to be in 1's complement form.

The exclusive OR may be used for code conversions, for example conversion from Gray to Binary and Binary to Gray. Figure 4a and 4b.

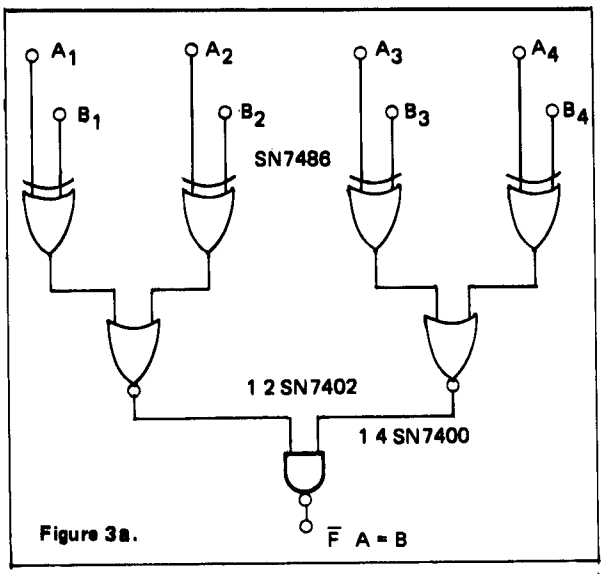


Figure 3a.

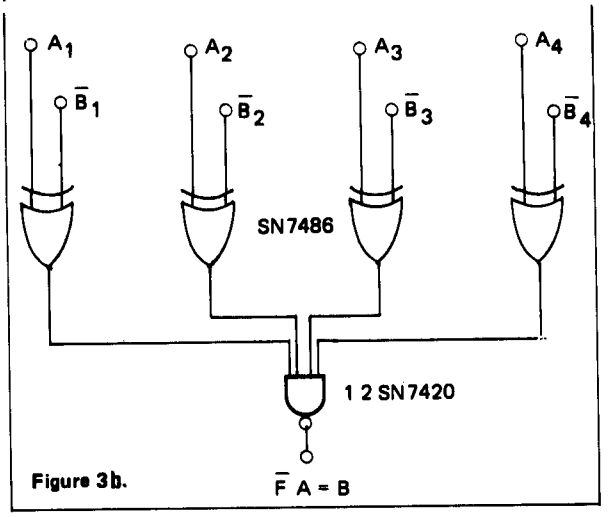


Figure 3b.

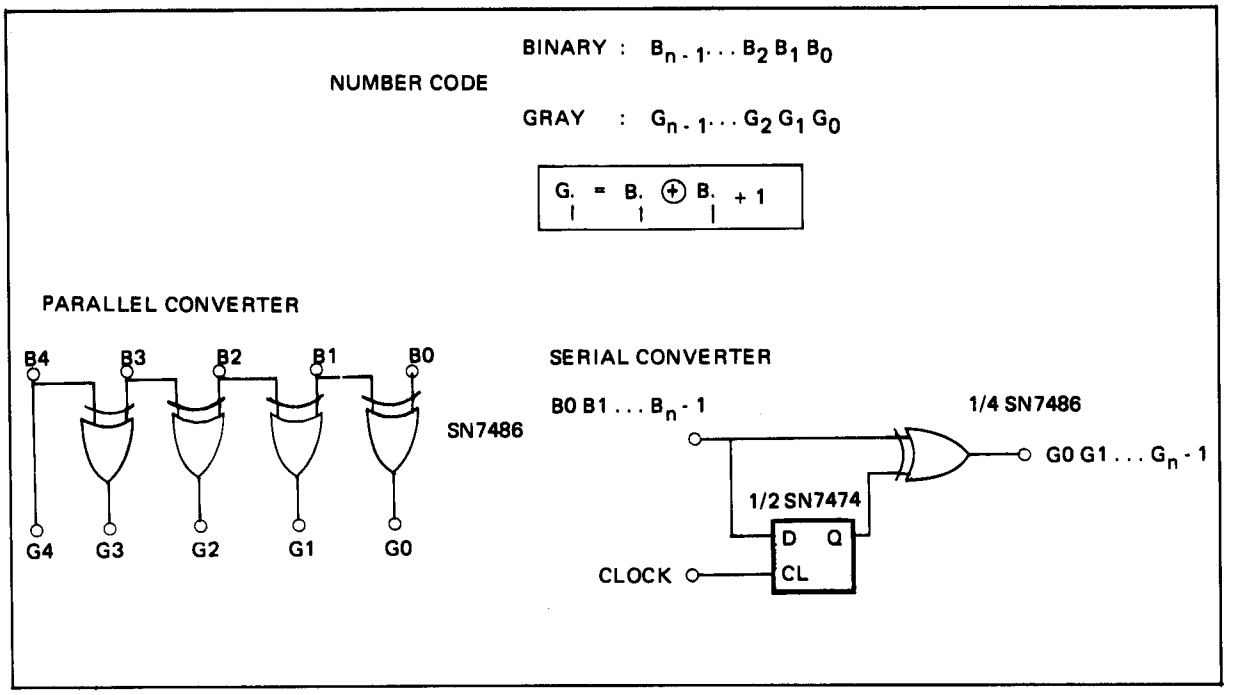


Figure 4a.

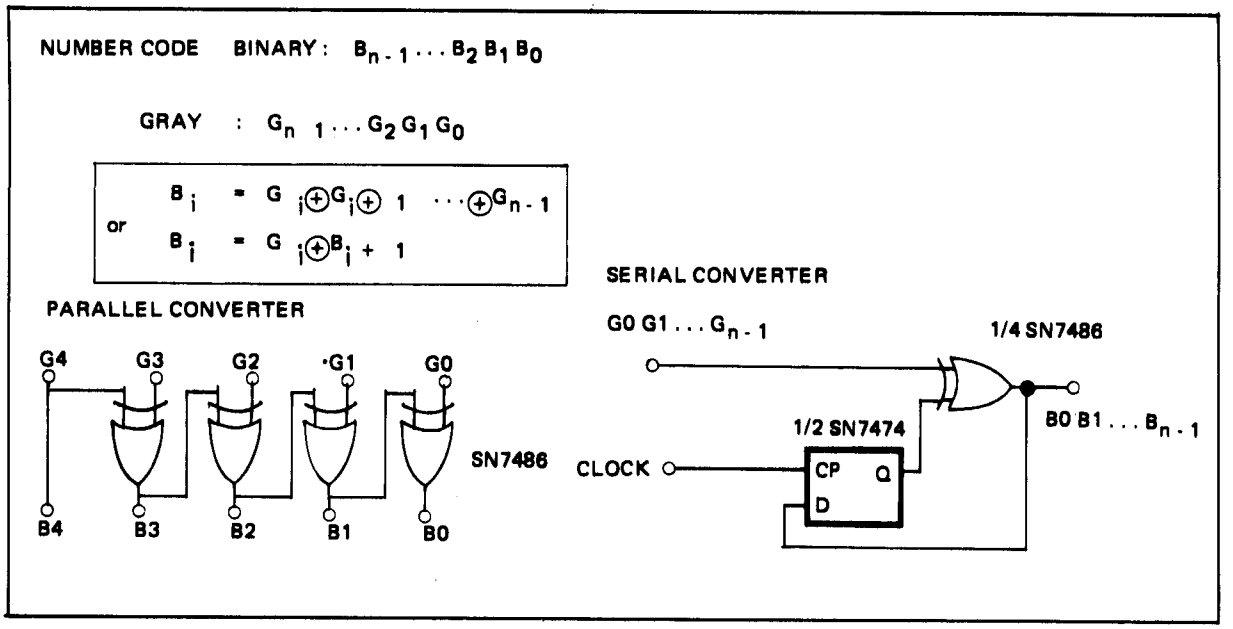


Figure 4b.

Parity Generation & Checking

By forming the modulo 2 sum of a number of data bits in a word, it is possible to determine if the word contains an odd or even number of ones (parity). If after transmission through a data link the word maintains the original parity then it cannot contain an error of 1 bit, it may however contain multiple errors that produce identical parity to the original word.

If more than single bit errors are to be detected and corrected 'Hamming codes' should be employed.

The SN74180 and SN74S280 are 9 bit odd/even parity generators, checkers. A simple parity checker using the SN74180 is shown in figure 5.

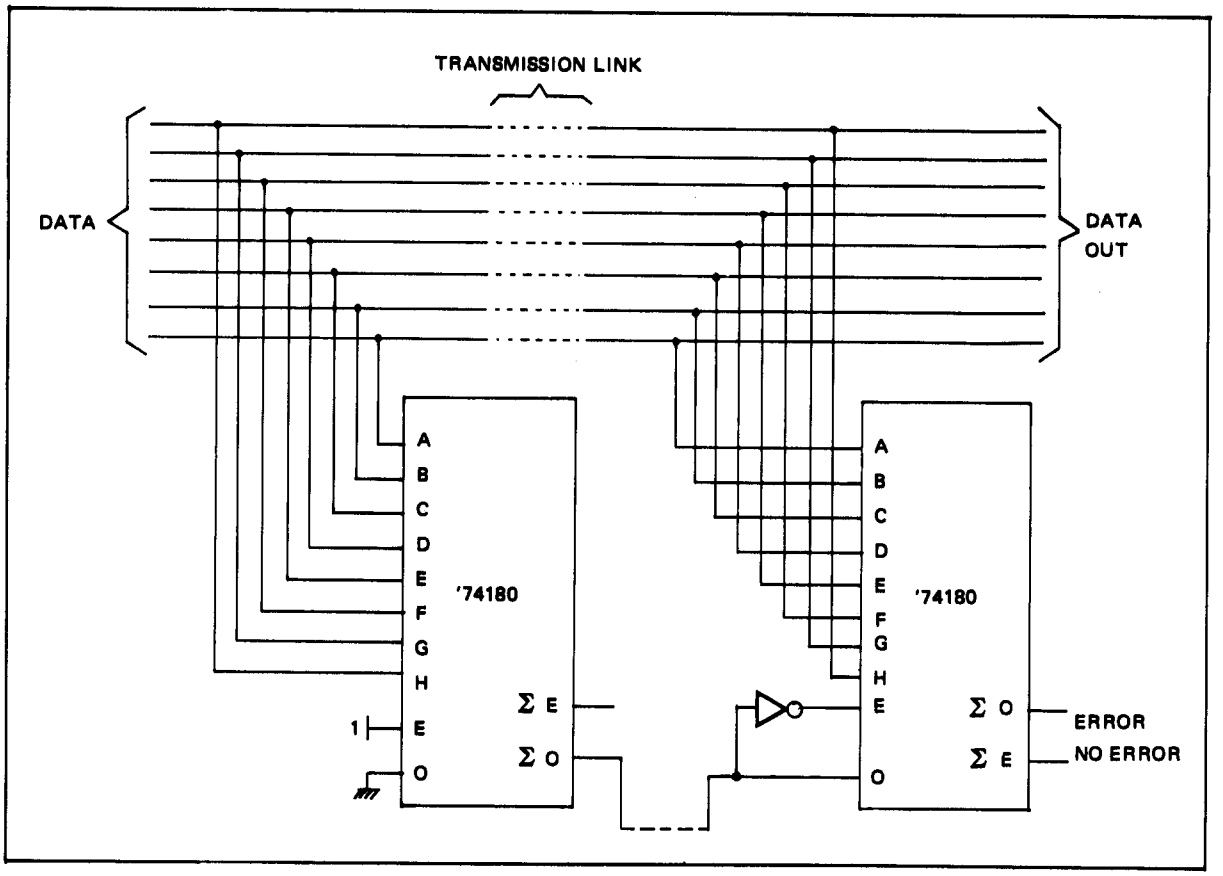


Figure 5. Data Error Detector

The system may be expanded to cover any number of data bits. Parity generators may be cascaded in two ways depending on the speed required. Figure 6 shows two methods by which additional inputs may be provided on the SN74S280 by using the SN74S86.

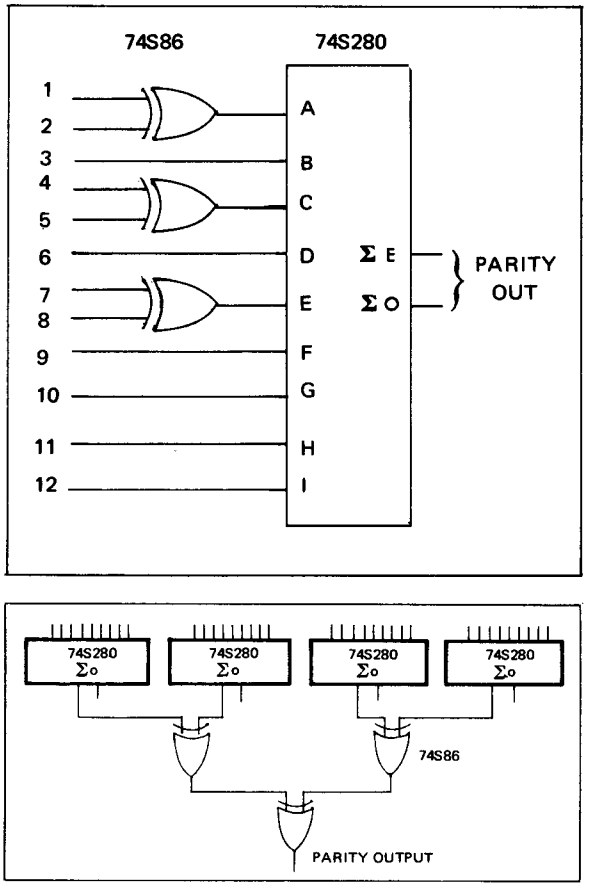


Figure 6.

For maximum speed with a large number of inputs are required the configuration shown in figure 7 may be used.

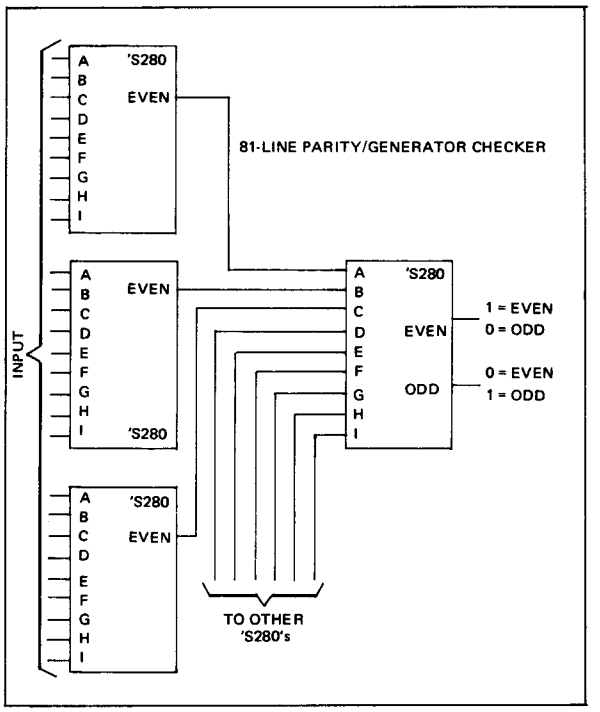


Figure 7.

This will generate parity for 81 bits within 25 ns. Alternatively, if extreme speed is not required parity generators may be cascaded as shown in figure 8.

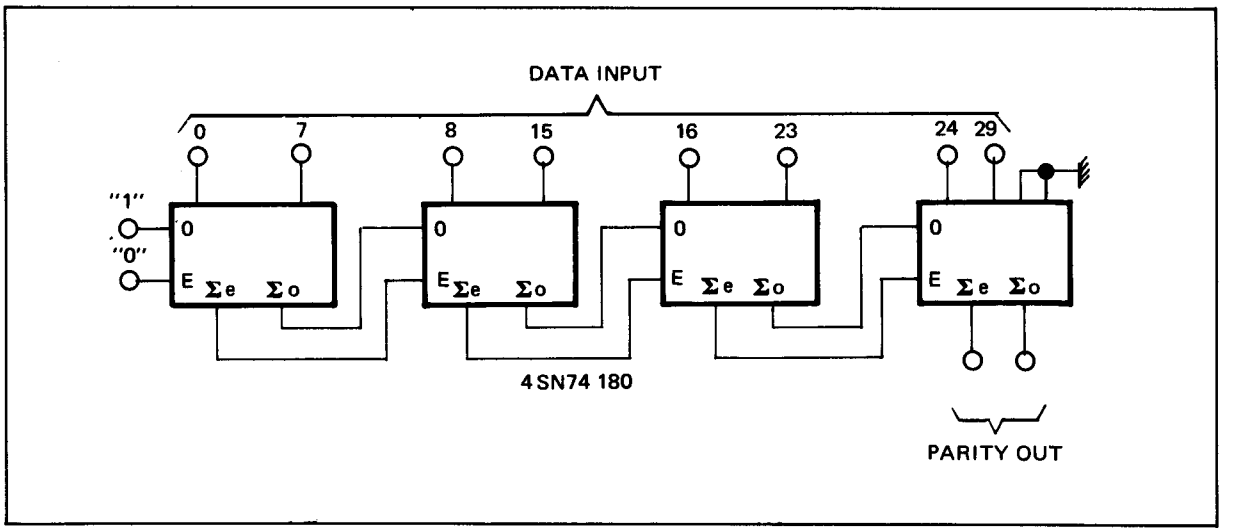


Figure 8.

An unusual application of parity generators is their use as modulo 2 adders for generating feedback functions for Pseudo Random Number Generators. A configuration that will generate cycle lengths from (2^2-1) to (2^8-1) is shown in figure 9.

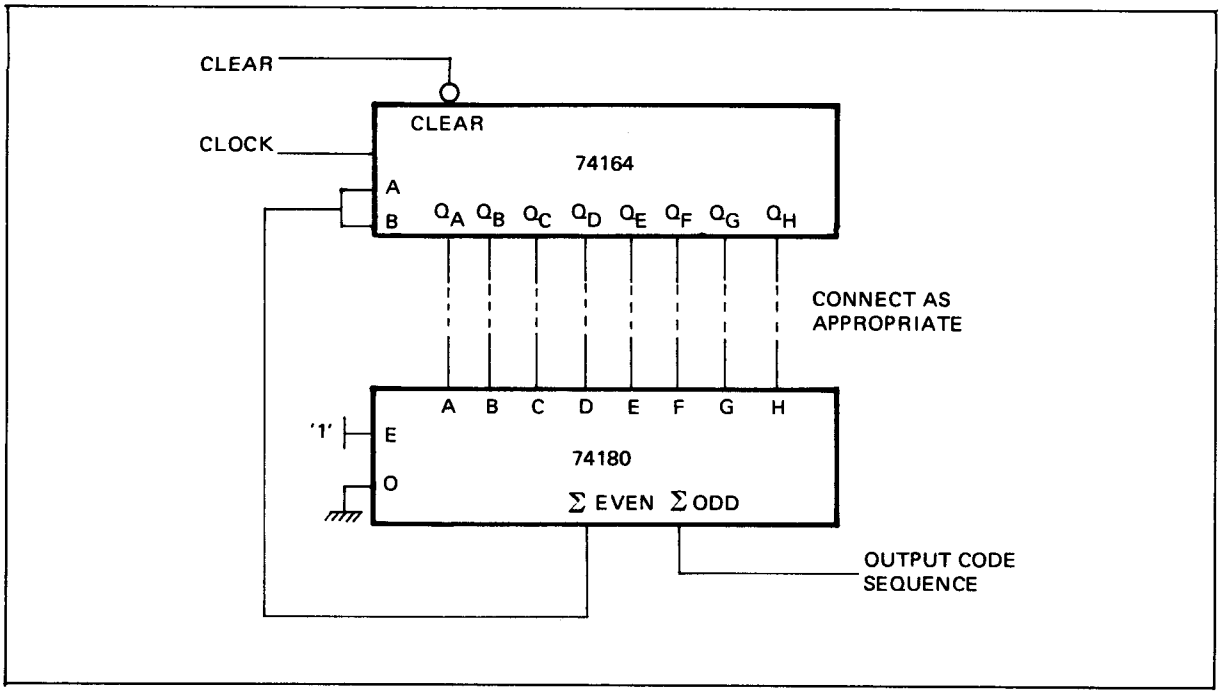


Figure 9.

As previously mentioned parity checks will indicate a single bit error but will not allow the erroneous data to be corrected. A method of overcoming this problem is to add additional check digits that are distributed throughout the message group in such a way as to provide parity checks on various digit positions. Such codes are known as Hamming codes. To correct an error, parity checks on the received data groups are made in order, a successful check being designated by an 0 and an error by a 1. The resulting binary number formed by these checks indicates the position of the error, which may then be corrected.

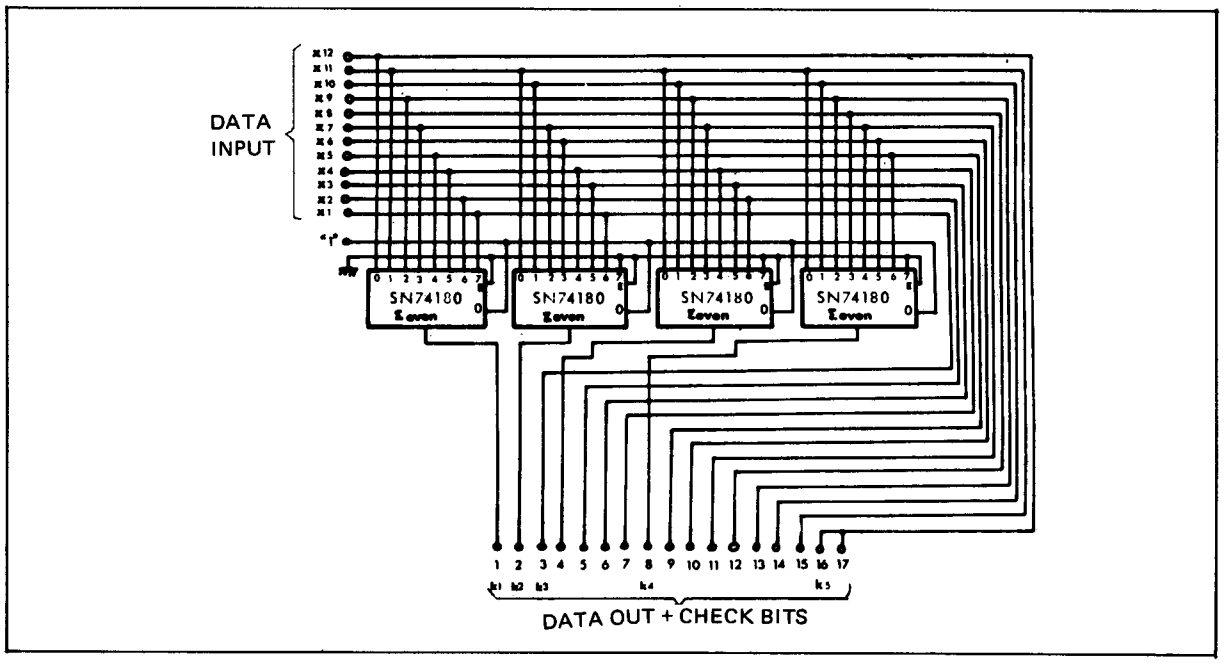


Figure 10a

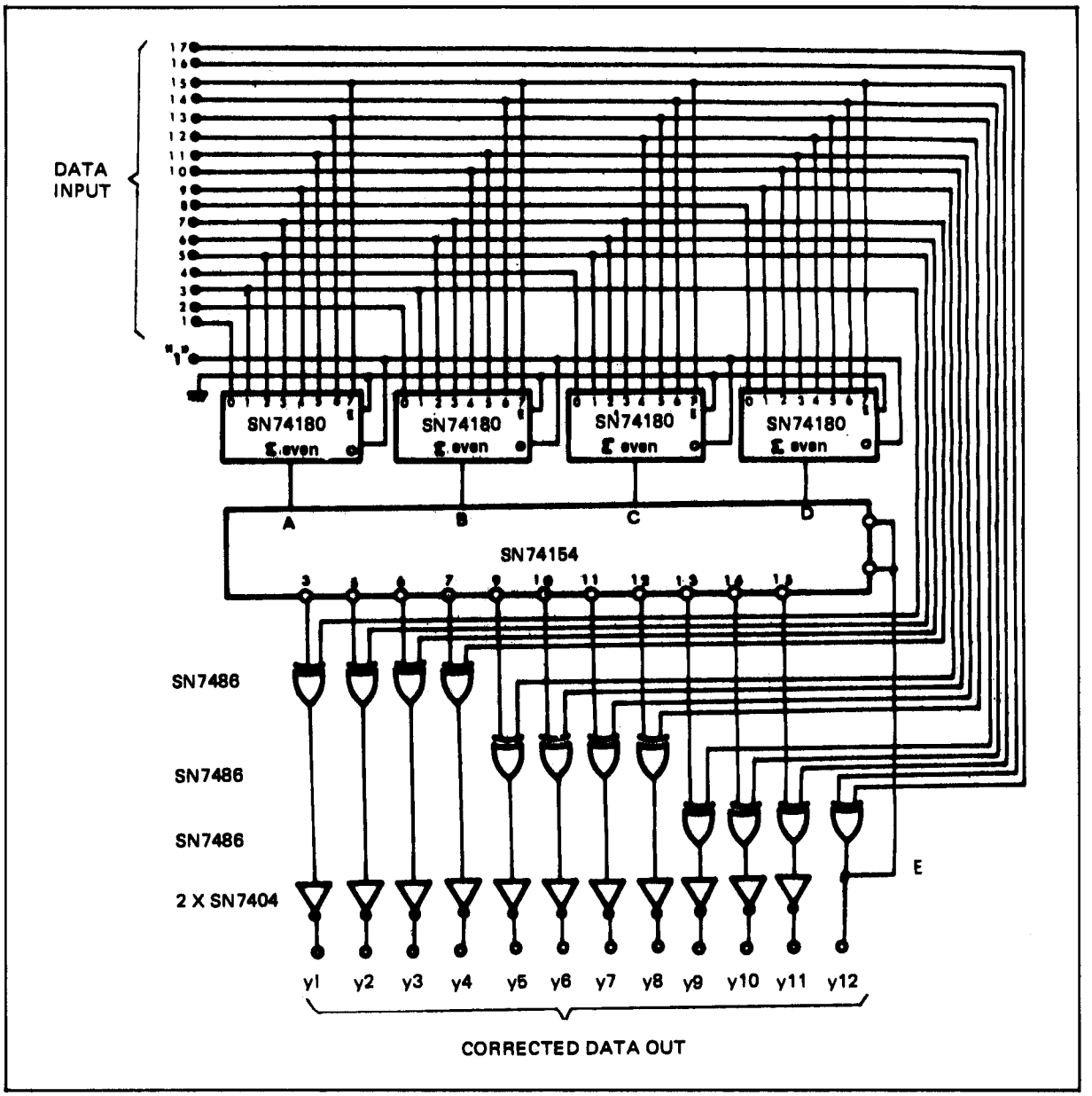


Figure 10b.

Figures 10a and 10b show a 12 bit Hamming Code generator and corrector. The 12 data bits have an additional 5 check bits inserted in positions 1, 2, 3, 8 and 16.

The decoder shown in figure 10b determines the error position and then inverts the erroneous bit, producing the correct data code at outputs Y1 to Y12.

Adders and Arithmetic Logic Units (ALUs)

It is difficult to show how arithmetic devices may be used in isolation, they generally form a part of a much larger system or subsystem. For example a fast adder tree may be used to sum the partial products developed by a parallel multiplier, which together with comparitors, may be used to generate reciprocals. The following application examples illustrate the use of some of the available arithmetic devices.

Figure 11 shows how the SN7483 four bit binary adder may be used for addition and subtraction in conjunction with the SN74H87 true-zero complement element. Subtraction is carried out by the addition of 2's complements. Negative values of a number X are represented by the 2's complement of X i.e. $(2^{n+1}-X)$, this when added to Y gives the result (Y – X).

i.e. $(2^{n+1}-X) + Y = (Y - X) + 2^{n+1}$

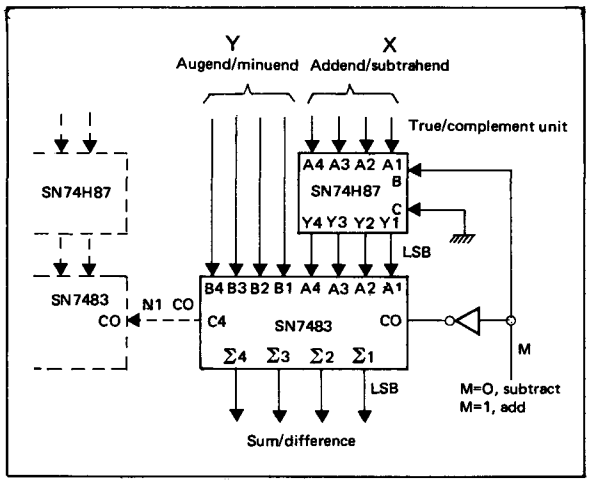


Figure 11.

The 2s complement of X is generated by interchanging the 1s and 0s in X and adding 1 to the result. The interchange is carried out by the SN74H87 and 1 is added at the carry input to the adder.

The 2^{n+1} term appears as a carry from the last adder stage and indicates that the result of the subtraction is positive (sign bit). When the sign bit is a zero the output represents a negative quantity and appears in 2's complement form.

Addition and Subtraction of Decimal Numbers with Binary Representations

In some instances it is desirable to perform arithmetic operations directly, using decimal numbers. This need often occurs in systems where the result of the arithmetic operation is to be displayed directly and it is desired to avoid code conversions. Two of the most used decimal arithmetic codes are Binary Coded Decimal (BCD) and Excess-3. For BCD the coding is identical to the equivalent binary numbers 0 to 9. Excess 3 code is similar to BCD except that an 'offset' of 3 is added to all decades, e.g. 99 is represented by 1100, 1100. This code has the advantage that it is self-complementing.

When two four bit BCD numbers and a possible carry from a previous decade are added, nineteen different sum digits can be produced. Of these only ten will be in correct BCD form, the remainder requiring some form of correction. To correct sums greater or equal to ten, it is necessary to subtract ten from the sum and produce a carry bit. The subtraction is carried out by the addition of the 2's complement of ten, i.e. 0110. Figure 12 shows how two four bit adders may be used for BCD addition.

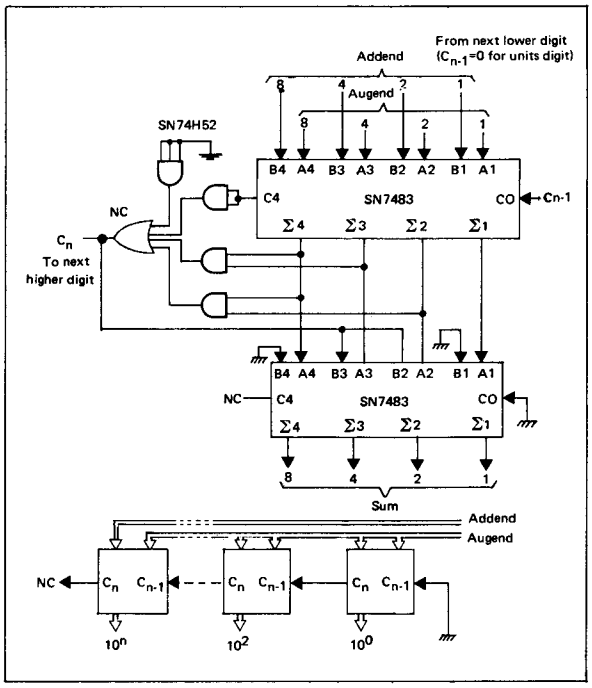


Figure 12.

The first adder adds the two BCD numbers as though they were in binary notation. If the resultant sum is equal to or greater than ten, which is detected by the SN74H52, binary six is added i.e. ten subtracted by the second adder. This method of adding a 'filler digit' to the sum from the first adder may be used to construct adders that operate to any base.

An example of a BCD adder being used to produce a reversible BCD counter is shown in figure 13. Here subtraction of one from the counter register is achieved by the addition of the 10's complement of one.

The same overall function could of course be obtained by using two reversible BCD counter packages, it does however illustrate how adders may be used.

BCD Subtraction

BCD subtraction is carried out by the addition of complements. The 10's or 9's complement may be used. It is generally easier to generate the 9's complement of a number X i.e. (9–X) and then the 10's complement (10–X) by adding one to the carry input of the adder.

Complement generation may be carried out by random logic as shown in figure 14 or by using part of a Read only Memory ROM such as the SN74184, figure 15.

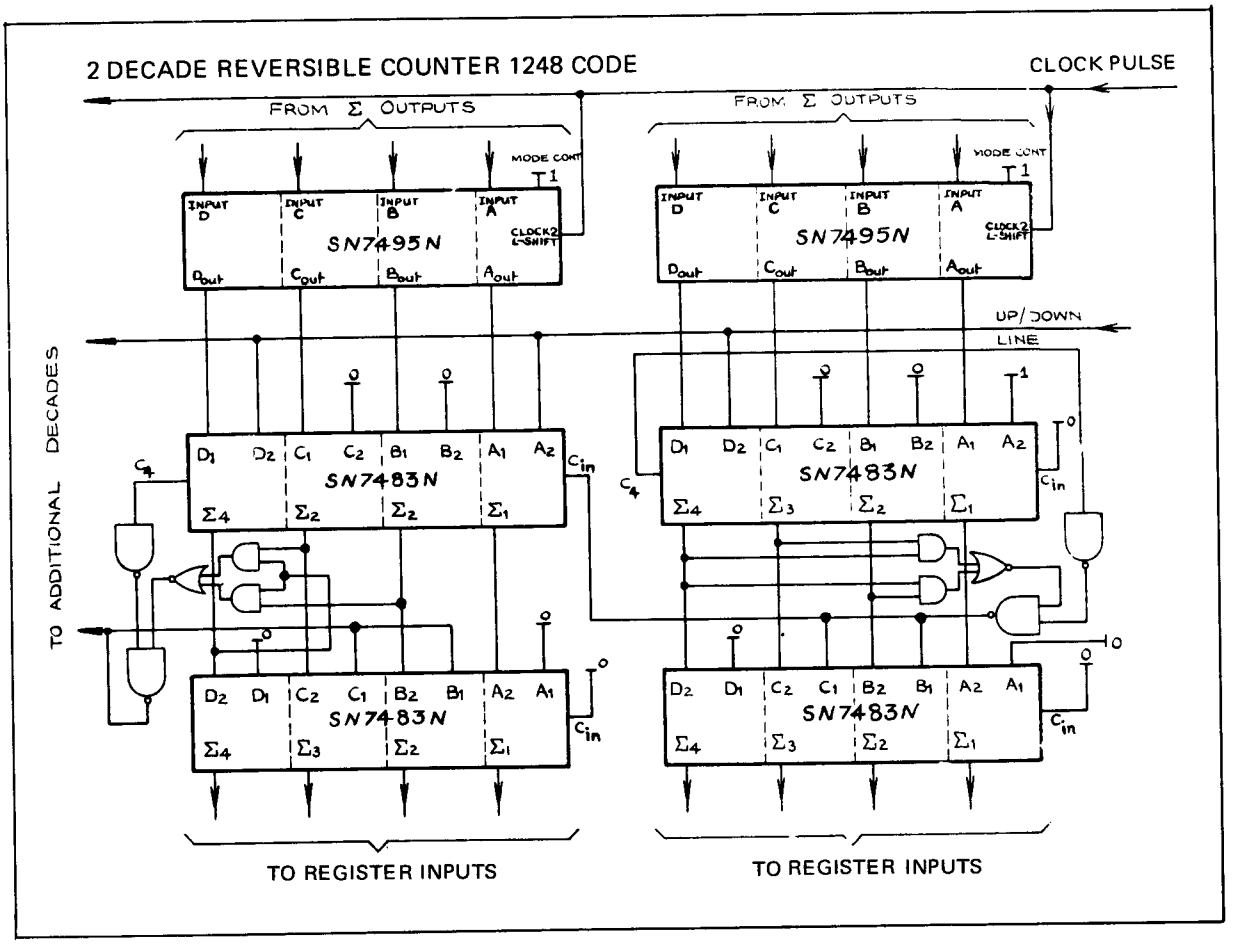


Figure 13.

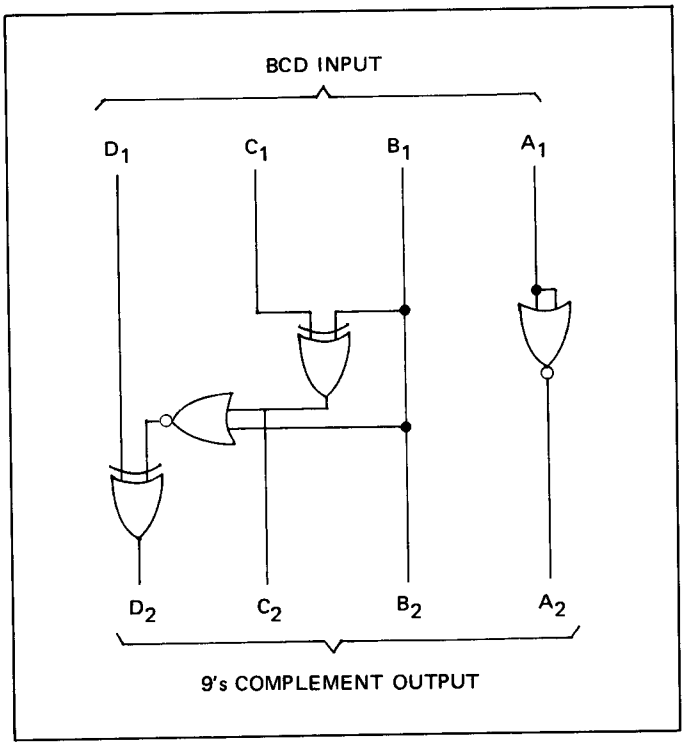


Figure 14.

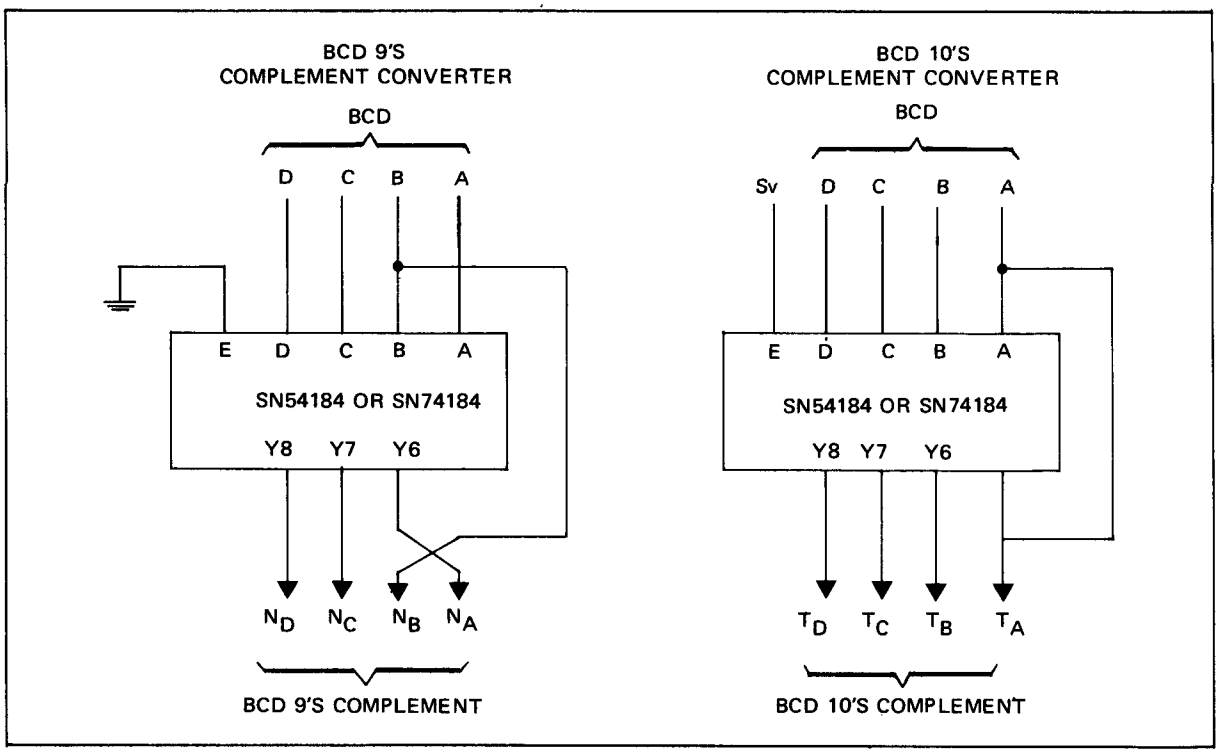


Figure 15.

FUNCTION TABLE
BCD 9'S OR BCD 10'S
COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated when it is high, the BCD 10's complement is generated.

Arithmetic Logic Units, Carry look ahead, and Carry save adders

Arithmetic Logic Units are building blocks that may be used for very high speed parallel data addition, subtraction, magnitude comparison and shifting etc. The function performed by the ALU is determined by logical control inputs. The SN74S181/181 will perform 16 binary arithmetic or 16 logic function operations on two 4 bit data words as shown in figure 16. The operation is selected by four function select lines (S0, S1, S2, S3). When used to perform arithmetic operations, as opposed to boolean functions, the internal carries from the adders must be enabled by taking the mode control low. When the mode control is high the device operates in the logic function mode.

ALU Signal Designations

The '181, 'LS181, and 'S181 can be used with the signal designations of either Figure 16A or Figure 16B.

The logic functions and arithmetic operations obtained with signal designations as in Figure 16A are given in Table 1 those obtained with the signal designations of Figure 16B are given in Table 2.

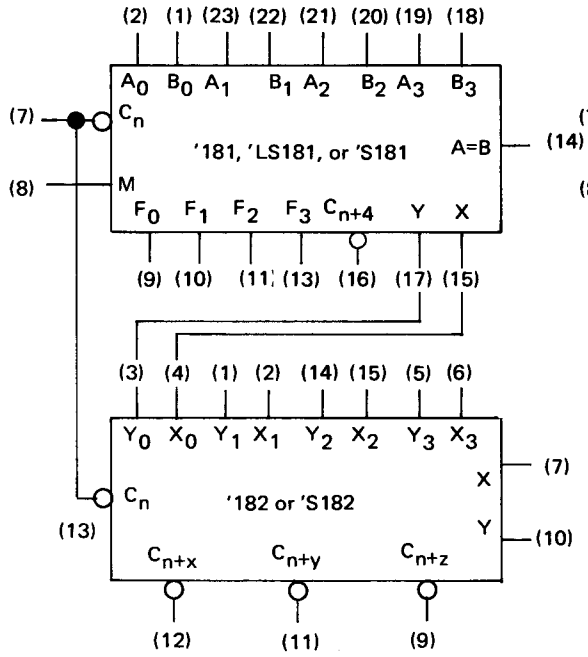


FIGURE 16a
(FOR TABLE 1)

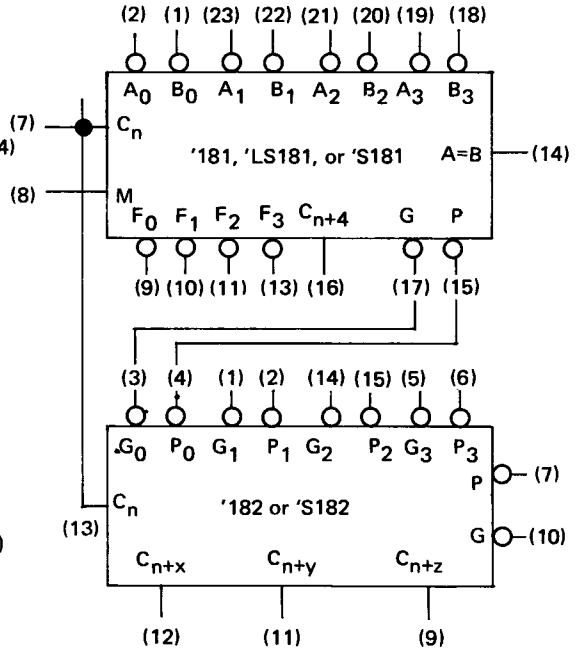


FIGURE 16b
(FOR TABLE 2)

TABLE 1

	ACTIVE-HIGH DATA		
	M = H	M = L; ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L L L L	$F = \overline{A}$	F = A	F = A PLUS 1
L L L H	$F = \overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L H L H	$F = \overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$ PLUS 1
L H H L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H L L L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	$F = A + \overline{B}$	$F = (A + B)$ PLUS A	$F = (A + B)$ PLUS A PLUS 1
H H H L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION	ACTIVE-LOW DATA		
	M = H	M = L; ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L L L L	$F = \overline{A}$	F = A MINUS 1	F = A
L L L H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L L H L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	$F = \overline{A + B}$	F = A PLUS $(A + \overline{B})$	$F = A$ PLUS $(A + \overline{B})$ PLUS 1
L H L H	$F = \overline{B}$	F = AB PLUS $(A + \overline{B})$	$F = AB$ PLUS $(A + \overline{B})$ PLUS 1
L H H L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
H L L L	$F = \overline{A}B$	F = A PLUS $(A + B)$	F = A PLUS $(A + B)$ PLUS 1
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	$F = A\overline{B}$ PLUS $(A + B)$	$F = A\overline{B}$ PLUS $(A + B)$ PLUS 1
H L H H	F = A + B	F = A + B	$F = (A + B)$ PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

The SN74S181 may be used with either active low or active high data. Compared with a conventional 4 bit adder three additional outputs are provided. An equality output, indicating when the two input words are identical, together with a carry propagate (P) and a carry generate (G) output. Why these outputs are generated and how they are used to speed up operations is best explained with reference to a simple adder stage. The truth table for such an adder is shown in figure 17.

INPUTS			OUTPUTS	
C_n	A_n	B_n	F_n	C_{n+1}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Figure 17.

The sum output F_n is expressed by $A_n \oplus B_n \oplus C_n$ the modulo 2 sum of the inputs. Carry output C_{n+1} is generated if 2 or all 3 of the inputs are present, therefore C_{n+1} may be expressed as;

$$C_{n+1} = A_n \cdot B_n + A_n \cdot C_n + B_n \cdot C_n$$

This boolean expression can be factored,

$$C_{n+1} = A_n \cdot B_n + C_n \cdot (A_n + B_n)$$

The first term is called a 'carry generate' condition in stage n.

$$G_n = A_n \cdot B_n$$

There will be a carry C_{n+1} if G_n is true *independent* of the input carry C_n, to stage n.

The term $A_n + B_n$ is called a carry propagate condition in stage n because a carry input C_n will be propagated through stage n and will generate a carry C_{n+1} *independent* of the sum F_n from stage n. When all the P and G terms are fed forward to more significant stages a full carry look ahead scheme between the four bits in a package can be achieved. Thus for n stages,

$n = 0 \quad C_0 = C_{in}$

$n = 1 \quad C_1 = G_1 + P_1 C_{in}$

$n = 2 \quad C_2 = G_2 + P_2 G_1 + P_2 P_1 C_{in}$

$n = 3 \quad C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_{in}$

This method allows a very fast carry to be produced by the ALU. This reasoning may be expanded to cover carry look ahead between ALUs by using the P_n and G_n outputs. If a 4 bit ALU package is called a group then the same logic equations that provide simultaneous carry between the bits within the group may be used for 'group level' look ahead. If the G and P outputs from 4 groups (*SN74S181s*) are fed into an SN74S182 then carry look ahead over 4 groups (16 bits) may be achieved. This method may be extended to produce carry look ahead over 3 levels. Various possible arrangements are shown in figure 18.

If the speed requirements for arithmetic functions are such that ripple carry between packages can be tolerated the output C_{n+4} can be fed directly into the C_{in} carry of the next package and no SN54182 package is required.

Subtraction is achieved by 1's complement addition. The 1's complement of the subtrahend is generated internal to the package. Subtraction times are in the same range as summation times. 1's complement arithmetic of course necessitates an "end around" carry or a 'forced' carry.

If two operands with equal magnitude are applied to the data inputs and the ALU is operated in the subtract mode (1's complement addition) all function outputs ($F_0 \ldots F_3$) will assume a logical '1' state. This state is decoded and logical equivalence is indicated at the COMP. output. This output has an open collector so that the compare function for the entire ALU can be achieved by wire-ANDing the COMP. outputs. By observing the carry outputs C_{n+4} in the subtract mode magnitude comparisons of the two operands can be made.

For active low operands: C_{n+4} High: $A < B$

C_{n+4} Low: $A > B$

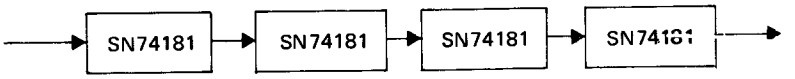
For active high operands: C_{n+4} High: $A > B$

C_{n+4} Low: $A < B$

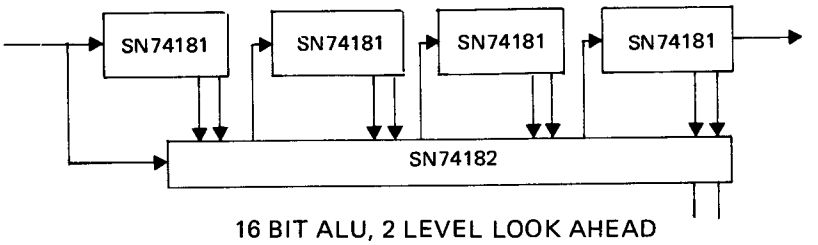
Besides the arithmetic sum and difference (and the comparison operation in the difference mode) a number of other useful arithmetic functions can be generated. (See Function Table). Some masking operations can also be performed internal to the device. Most noticeable the operand A can be decremented by one or shifted to the left by one position (A plus A).

Logic Functions

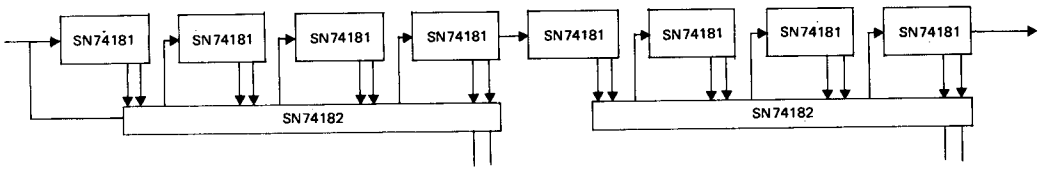
When the carry between bits and packages is inhibited all possible 16 logic functions of the 2 bits A_n, B_n can be generated according to the control inputs $X_0 \ldots X_3$. This implies that the operands can be transferred to the outputs without any arithmetic or logic manipulation, $F_n = (A_n, \bar{A}_n, B_n, \bar{B}_n)$ and that the outputs can be held independent of the inputs to all zero or all one states $F_n = 0, 1$.



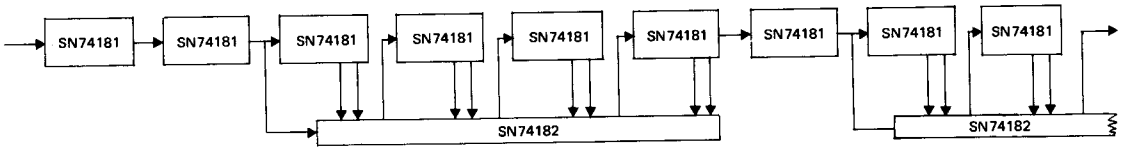
16 BIT ALU, RIPPLE CARRY



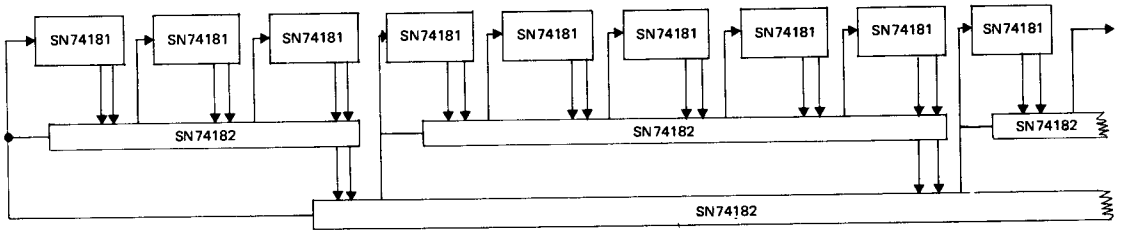
16 BIT ALU, 2 LEVEL LOOK AHEAD



32 BIT ALU, 2. LEVEL LOOK AHEAD OVER 16 BIT GROUPS



COMBINED 2 LEVEL LOOK AHEAD AND RIPPLE CARRY ALU



64 BIT ALU, FULL CARRY LOOK AHEAD IN 3 LEVELS

Figure 18.

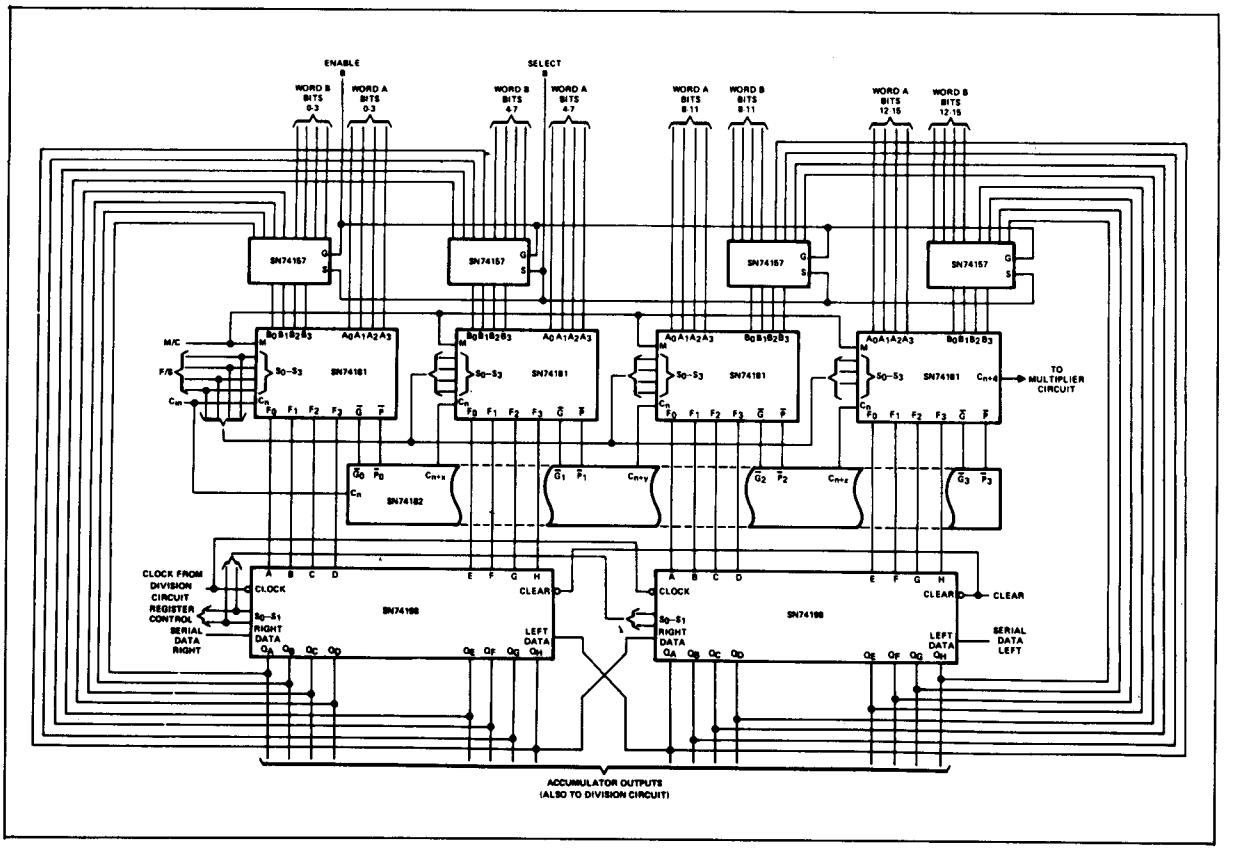


Figure 19. 16-BIT HIGH-SPEED PARALLEL ACCUMULATOR WITH FULL LOOK-AHEAD

High Speed Accumulator using ALUs.

The high speed parallel accumulator shown in figure 19. features full look ahead to reduce the typical add time to 36 nanoseconds and the typical subtract time to 40 nanoseconds through the arithmetic logic unit (ALU) and the look-ahead carry generator. Used in conjunction with the quadruple two-input multiplexers and the eight-bit parallel-access shift registers the total times are typically 88 nanoseconds for addition and 92 nanoseconds for subtraction.

The arrangement shown in figure 19 provides for high speed processing of arithmetic operations. As the SN74198 is a bidirectional shift register, some multiplication (and power-of-two division) steps can be made with a simple shift-left or shift-right operation. In addition, complete arithmetic capability is provided as the accumulator outputs are multiplexed with and may be selected as the B input to the ALU's with the result that successive additions are performed with minimal delays.

Addition or subtraction

a. Clear and set register for parallel load (register control inputs = 1,1.)
b. Select and enable the word B input multiplexers.
c. With ALU mode control (M/C) low, set function select (F/S) for addition (1001) or subtraction (0110).
d. Apply words A and B, clock the register, and read sum or difference at accumulator output.

Two methods are available for handling the carry for subtraction:

a. A forced carry input, the fastest method, produces the two's complement of negative answers.
b. The end-around carry produces the one's complement of negative answers.

Division

Division is accomplished by successively subtracting the divisor from the dividend and counting the number of successive subtractions to obtain the quotient, see figure 20.

When no remainder exists, the cycle is terminated by detecting all zeros at the accumulator outputs and the content of the counter is the quotient.

A remainder is detected when C_{n+4} goes low causing the 16-bit binary counter clock to be inhibited. When this situation exists the quotient is again read from the 16-bit counter and the remainder is read from the accumulator.

Multiplication

To multiply A by 2:

a. Clear and set register for parallel load (register control inputs = 1, 1.)
b. With ALU mode control low, set function select for A plus A (S0 = 0S1 = 0S2 = 1 S3 = 1).
c. Apply word A, clock the register, and read 2A at accumulator output.

To multiply A by 3:

a. Multiply A by 2 as above.
b. Select and enable the accumulator outputs to supply the ALU B inputs.
c. Change function select to add (S0 = 1. S1 = 0, S2 = 0, S3 = 1), clock and register, and read 3A at accumulator output.

To multiply A by 4:

a. Multiply A by 2 as previously explained.
b. Change register control to shift in direction of most significant bit.
c. Clock the register once and read 4A at accumulator output.

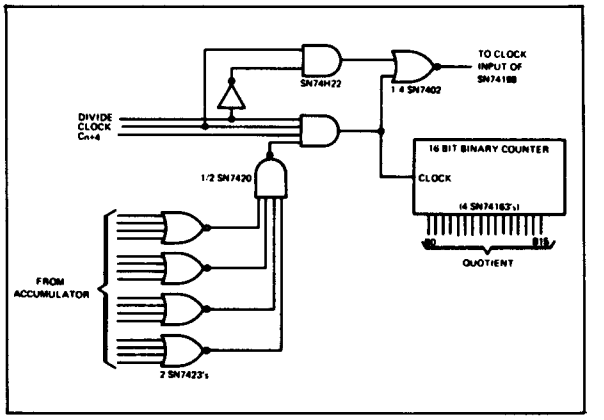


Figure 20. DIVISION CIRCUIT

Carry Save Adder

'Carry save' adders are used where it is necessary to generate the carry term at the same time as the sum. They nearly always employ high speed parallel logic. An example using the SN74H183 dual carry save adder as an M out of N code detector is shown in figure 21.

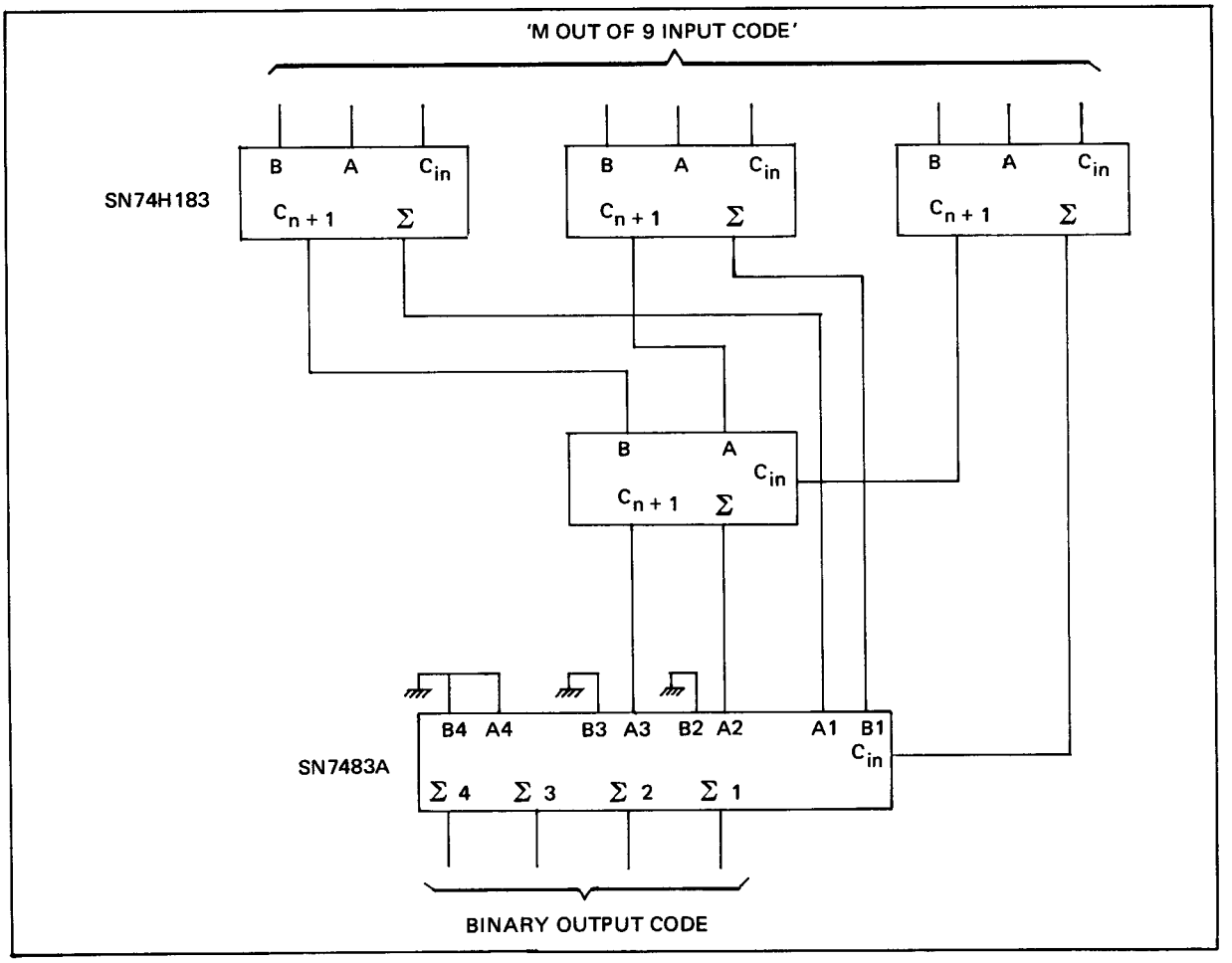


Figure 21.

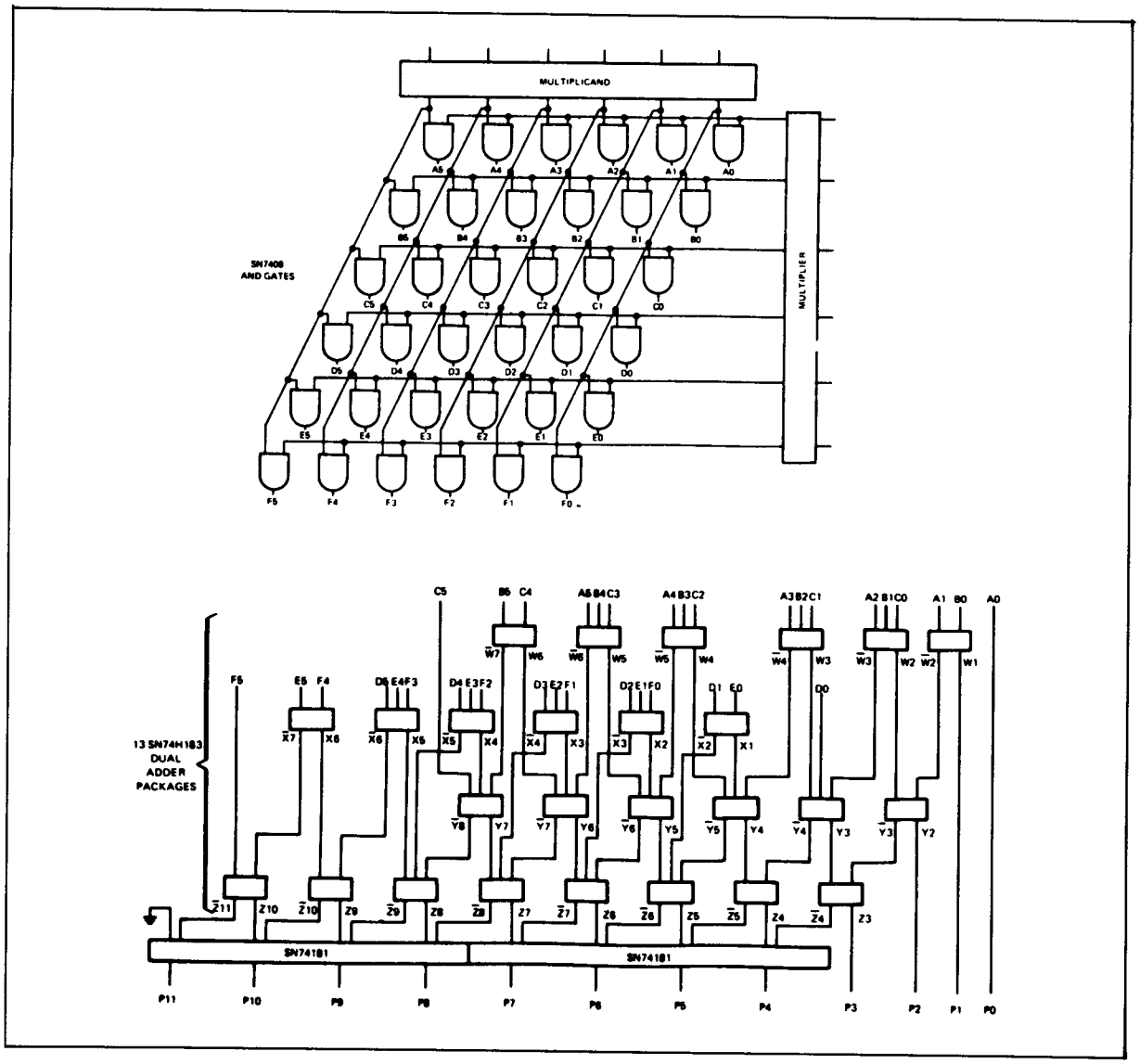


Figure 22. IMPLEMENTATION OF A HIGH-SPEED MULTIPLIER FOR TWO 6-BIT BINARY WORDS

Each input to the adder tree has a 'weighting' of one. The weighted inputs are successively combined to produce a Binary weighted output from the final adder. The binary number represents the number of inputs that are present out of a possible total of 9.

Binary Multiplication using Carry Save Adders

Figure 22 shows how carry save adders may be used to produce a high speed 6 bit binary multiplier. A numerical example is shown in figure 23 which shows how 55 would be multiplied by 45.

Binary multiplication can be expressed as a two step operation: ANDing the multiplicand with the multiplier one bit at a time, and adding. Furthermore, since adding is commutative (not dependent on the order in which made) the ANDed subproducts can be combined in any order that observes the binary weight of each bit.

Another fact, not so obvious, is that groups of multiplier and multiplicand bits can also be ANDed, summed, and combined. As Figure 23 shows, the effect is the same whether the bits are ANDed and summed in complete groups, or whether they are ANDed, summed in subgroups, and then the subgroups added. The only difference is in the way the subproducts are added, due to the difference in the weight accorded the binary bits in each method. 'Weight' means the exponent or power of each bit; for example, if the MSB in a 4 bit multiplicand (2^3) is ANDed with the 2nd bit (2^1) in a multiplier, the result is a ($2^3 \times 2^1 = 2^3 + 1 = 2^4$) 2^4 bit (or 4th power bit).

The basic concept of the Wallace adder scheme is to consider carry outputs as sum bits of a higher order; that is, a carry in the 2^N column of binary bits is treated as a 2^{N+1} binary sum bit. This results in the generation of two groups of outputs; a carry

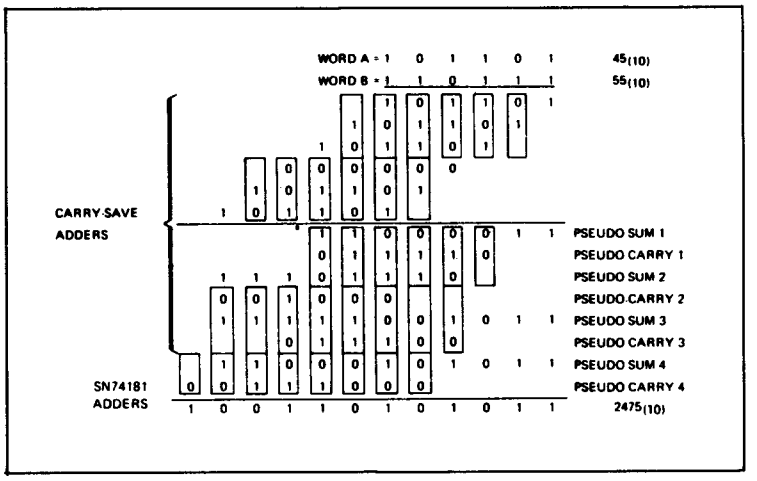


Figure 23.

group and a sum group. The SN74H183 is ideal for this application since the carry and sum propagation delays are identical. Because the carry and sum groups must be combined, a high speed adder using the SN74 181 ALU and 74 182 look-ahead carry generator that will accumulate the groups is used.

Performing Arithmetic functions with Read Only Memories (ROMs)

TTL Read Only Memories can be used effectively to perform high speed multiplications. For example, by programming two 1024 bit ROMs such as the SN74187, a binary 4 bit x 4 bit multiplier can be fabricated as shown in Figure 24. These ROMs are available as catalogue products as the SN74284 and SN74285.

Consider multiplications using ROMs, in which 4 bit x 4 bit products will be considered as subproducts for larger numbers. After the subproducts are developed, high speed multiplication requires that a fast addition scheme be used to sum these subproducts. The carry save tree can be used here and is best accomplished with the Wallace adder scheme. When using ROMs, almost any TTL adder can be used to combine subproducts, such as the SN74283 four bit full adder, which will give minimum package counts, or carry save trees in which the SN74H183 carry save adder is employed to give the best propagation delays.

Figure 25 shows a 16 bit x 16 bit multiplier with a SN74H183 Wallace tree network, SN74S181, SN74S182 carry look-ahead adder, SN74284 and SN74285 multiplier chips, and featuring a 32 bit product in (typically) 103 nanoseconds.

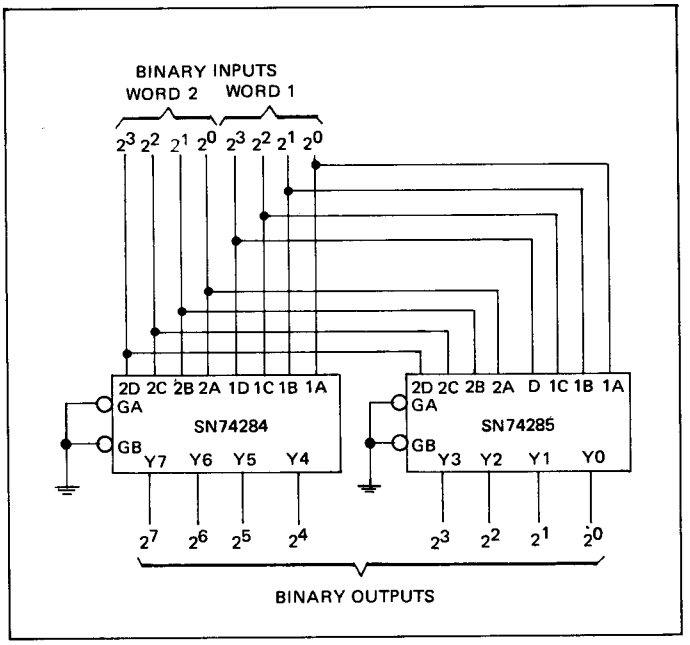


Figure 24.

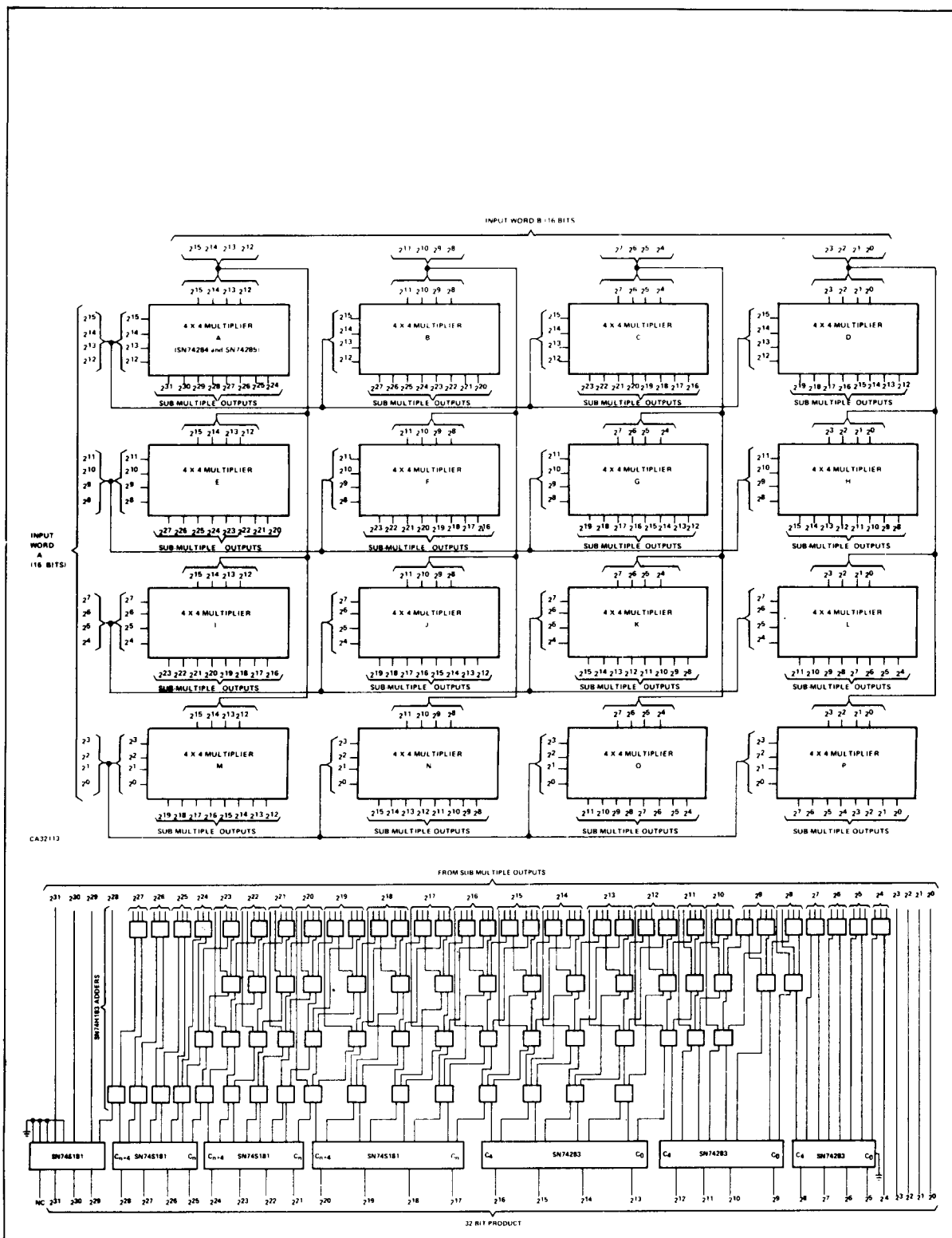

INPUT WORD B (16 BITS)
4 X 4 MULTIPLIER
A
(SN74284 and SN74285)
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
SUB MULTIPLE OUTPUTS
INPUT WORD A (16 BITS)
CA32113
FROM SUB MULTIPLE OUTPUTS
SN74H183 ADDERS
SN74S181
SN74S283
32 BIT PRODUCT

Figure 25.

Monostables

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	NO. OF INPUTS		OUTPUT PULSE RANGE	TYP TOTAL POWER DISSIPATION	DEVICE TYPES	NO. OF PINS
	POSITIVE	NEGATIVE				
SINGLE	1	2	40 ns–28 s	90 mW	SN74121	14
	1	2	40 ns–28 s	40 mW	SN74L121	14

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	NO. OF INPUTS		DIRECT CLEAR	OUTPUT PULSE RANGE	TYP TOTAL POWER	DEVICE TYPES	NO OF PINS
	POSITIVE	NEGATIVE					
SINGLE	2	2	Yes	45 ns–∞	115 mW	SN74122	14
	2	2	Yes	90 ns–∞	55 mW	SN74L122	14
DUAL	1	1	Yes	45 ns–∞	230 mW	SN74123	16
	1	1	Yes	90 ns–∞	115 mW	SN74L123	16

MONOSTABLES

The '121 devices are non-retriggerable monostables and the '122s and '123s retriggerable.

The '121 has two negative edge triggered inputs and one positive edge Schmitt-trigger input. The former expect a typical TTL transition while the latter will give a jitter free output pulse from a ramp. The output pulse width is compensated for variations of temperature and V_{CC}, giving a device which has a very good stability.

Apart from not being retriggerable, it has no clear facility and loses its accuracy for high duty cycles. A clear can be added externally as shown in Figure 1.

The longest time that can be obtained with the '121 is determined by the maximum allowable timing resistor and capacitor. To get a longer time the circuit in Figure 2 can be used.

The '122 and '123 are retriggerable monostables having clear inputs. The '122 has two positive and two negative transition triggering inputs, while the '123 which is dual, only has one of each for each half. In both types the clear is also gated with the inputs so that removing the clear signal can, for certain conditions of the inputs, trigger the monostable again.

The '122 and '123 will operate up to 100 percent duty cycle or thereabouts.

If the clear is used with a timing capacitor of greater than 1000pF then a diode must be used in series with the C_{ext}/R_{ext} terminal as shown on the data sheet. This allows a short clear pulse to reset the device and then be removed before the capacitor has been recharged. The diode however modifies the timing equation and reduces the maximum allowable value of R_T. The pulse width will also be more temperature sensitive.

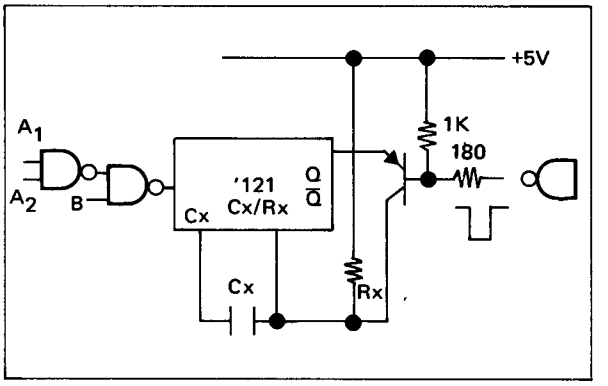


Figure 1.

The diode is also suggested for use with electrolytic capacitors which will not tolerate being reverse biased by more than 700 millivolts. The possible current is limited to less than 200μA.

The timing resistor can be increased above the data sheet maximum value by using a transistor in a similar circuit to that used with the '121. This is shown in Figure 3.

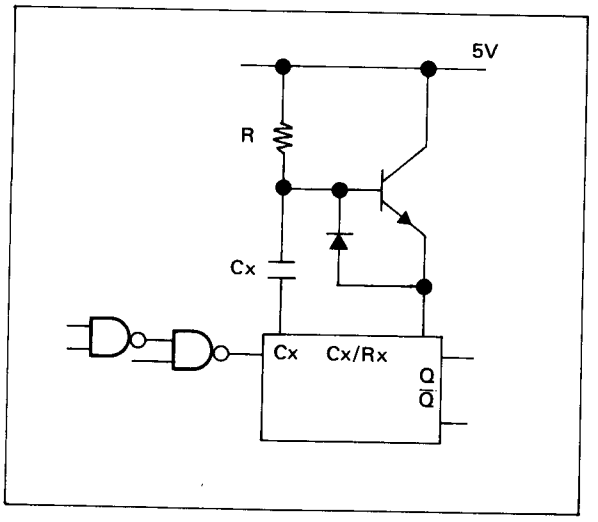


Figure 2.

The pulse width will be slightly longer than 0.7 CR and it will be temperature sensitive. R can be $h_{FE} \cdot R_{max}$ so the maximum value for R will be a megohm or two. But notice that the actual pulse width is h_{FE} independent.

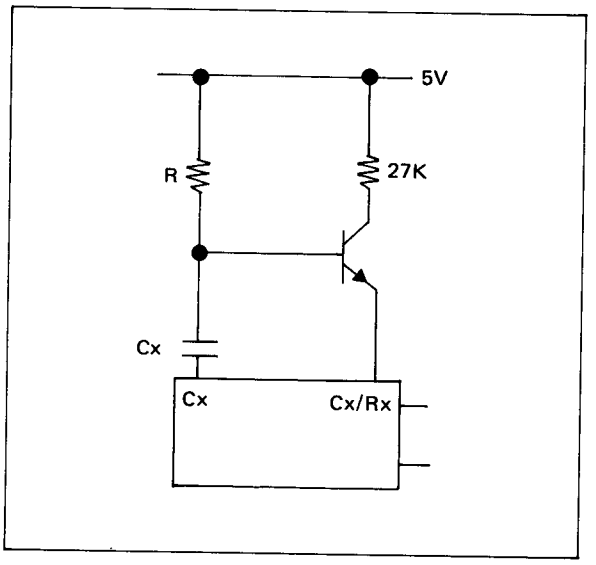


Figure 3.

The timing equation is similar to that with the diode.

One of the useful functions that can be made with the retriggerable monostables is an oscillator. Oscillators can be made easily and cheaply using one of the Schmitt trigger gates ('13, '14 or '132). One drawback is that the timing resistor is limited to about 390 ohms. This means two things. The frequency can only be adjusted by changing the capacitor and as the resistor is small the timing capacitor must be large for low frequencies.

Using a '122 or '123 as in Figure 4 avoids these problems.

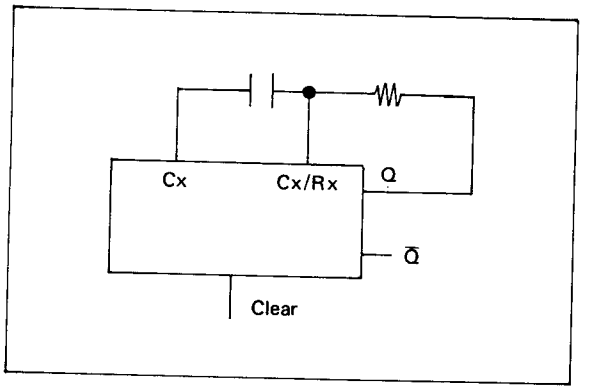
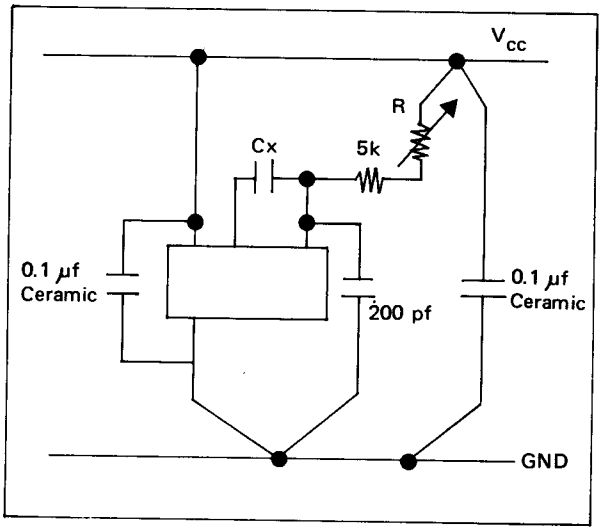


Figure 4.

The clear input can act as an enable/inhibit. The state of the other inputs is immaterial, all high gives the lowest power dissipation.

The rise and fall times of all input signals should meet the normal TTL requirement of better than 50ns. If input waveforms are slow the devices may trigger on the wrong edges (as well as the correct ones). The noise immunity at the inputs is the same as other TTL. If noise is affecting a device it is usually getting in at the R_X/C_X timing pin, which is a high impedance and it will terminate the output pulse prematurely. It is not likely to fire the monostable. A couple of hundred picoFarads can decouple the R_X/C_X pin without affecting the timing if C_X is much larger. The timing resistor should be as close to the device as possible and decoupled at the rail. Where a variable resistor with long leads is used as a front panel control it is better to put 5K or more of it close to the package and the rest in the control.



Suggested Layout

Figure 5.

Applications of Interface Devices

Line Drivers and Receivers

LINE CIRCUITS

LINE DRIVERS

TYPE	SN75109	SN75110	SN75150†	SN75450A
* Operating Frequency	> 10 MHz	> 10 MHz	10 kHz at 2500-pF Load	< 1 MHz
* Type of Lines	Balanced or Single-Ended	Balanced or Single-Ended	Single-Ended	Balanced or Single-Ended
* Length of Line	Up to 5,000'	Up to 10,000'	Up to 500'	Up to 500'
* Input	TTL	TTL	TTL	TTL
* Output	Current Mode	Current Mode	Voltage Mode	Current Mode
* Party Line Operation	Yes	Yes	No	Yes
* Strobe Control	Yes	Yes	No	
* Power Supply	+5 V and−5 V	+5 V and−5 V	+12 V and−12 V	+5 V
* No. of Pins	14	14	N = 14 P = 8	14

LINE RECEIVERS

TYPE	SN75107A	SN75108A	SN75154
* Input Sensitivity, Max	25 mV	25 mV	
* Switching Time, Max	25 ns	25 ns	50 ns
* Strobe Capability	Yes	Yes	No
* Output	TTL, Active Pull-Up	TTL, Open-Collector	TTL, Active Pull-Up
* Fan-Out	10	10	10
* Power Supply	+5 V and−5 V	+5 V and−5 V	+5 V or +12 V
No. of Pins	14	14	16
Application Notes			

† Satisfies requirements of EIA standard RS-232-C

SERIES LINE DRIVERS & RECEIVERS

General Considerations

1. All inputs of any device must be connected to something. In the case of unused parts of multi-channel devices the strobes or inhibit inputs and the logic inputs must be connected to ground or the nominal input voltage, via a resistor, as the truth table of the device and your system dictate. Failure to do so may cause a malfunction of the parts of devices which are used.
2. Where strobing or inhibiting are not required in the system concept, then inputs which will allow the driver or receiver to function MUST be provided. Failure to do so may cause an uncertainty at the output of the device.
3. In systems which are subject to noisy environments, it is advisable to bias one input of each line receiver, or one of the lines, at a voltage which can be overcome by a required signal but not by the general noise level – this will reduce chatter at the output of the receiver to a minimum.

N.B. In the above it has not been possible to give the exact voltages required as these vary from system to system, however, wherever connection to a voltage is required, this should be made via a resistor, (a 1kΩ resistor should be suitable in most applications).

4. Some users have adopted the practice of disabling line receivers by disconnecting power supplies, this practice should not be used unless the system concept dictates, and if it is adopted, special precautions, and in some cases alternative devices, are required. In these circumstances further assistance can be obtained from Texas Instruments Ltd.
5. Transmission lines should always be terminated, at both ends, in the Characteristic Impedance of the line. In the case of coaxial lines a single resistor between the inner and outer conductors is all that is required. In the case of twisted pair lines, for differential data transmission, each wire of the twisted pair should be connected to earth via a resistor of a value of half the Characteristic Impedance. For both party-line and single channel transmission lines, it is only necessary to have a termination at each extreme end of the line.
6. In party-line systems the number of receivers which can be attached to the line is governed by the following criteria:-

Length of Line	– attenuation and noise pick-up
Type of Line	– Characteristic Impedance and noise immunity
Type of Driver	– output power
Type of Receiver	– sensitivity and threshold voltage.

Applications of SN75107

One-Channel Balanced Transmission System:- SN75107 Series dual line circuits are designed for use in high-speed data transmission systems that utilize balanced, terminated transmission media such as twisted pair lines. Such a system operates in the balanced mode, so that any noise induced on one line is also induced in the other. The noise appears as common-mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and line receiver is not part of the signal circuit, so that system performance is not affected by circulating ground currents and ground noise.

The unique output circuit of the driver allows terminated transmission lines to be driven at normal line impedances. High-speed operation of the system is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized because of the low signal amplitude, low line impedances, and because the total current in a line pair remains constant.

A basic balanced transmission system using SN75107 Series devices is shown in Figure 1. Data is impressed on the twisted-pair line by unbalancing the line voltages by means of the driver output current. Line termination resistors labelled R_T are required only at the extreme ends of the line. For short lines, termination resistors only at the receiver end may prove adequate. Signal phasing depends on the driver output and receiver input polarities on the line.

Party-Line Balanced Systems: The need to communicate between many receivers and line drivers using the scheme in Figure 1 could require large amounts of wire and consequently increase the installation costs. For example, in transmitting and receiving information from the cockpit of an airplane to some remote area in the tail of the plane, the wire required for a multi-channel system might well weigh more than all of the equipment involved. Thus a method for sharing a single transmission line by several drivers and receivers is desirable.

The strobe feature of the receivers and the inhibit feature of the drivers allow SN75107 Series dual line circuits to be used in party-line (also called data-bus) applications. Examples are shown in Figure 2, 3, and 4. In each of these systems, an enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data can therefore be time-multiplexed on the transmission line.

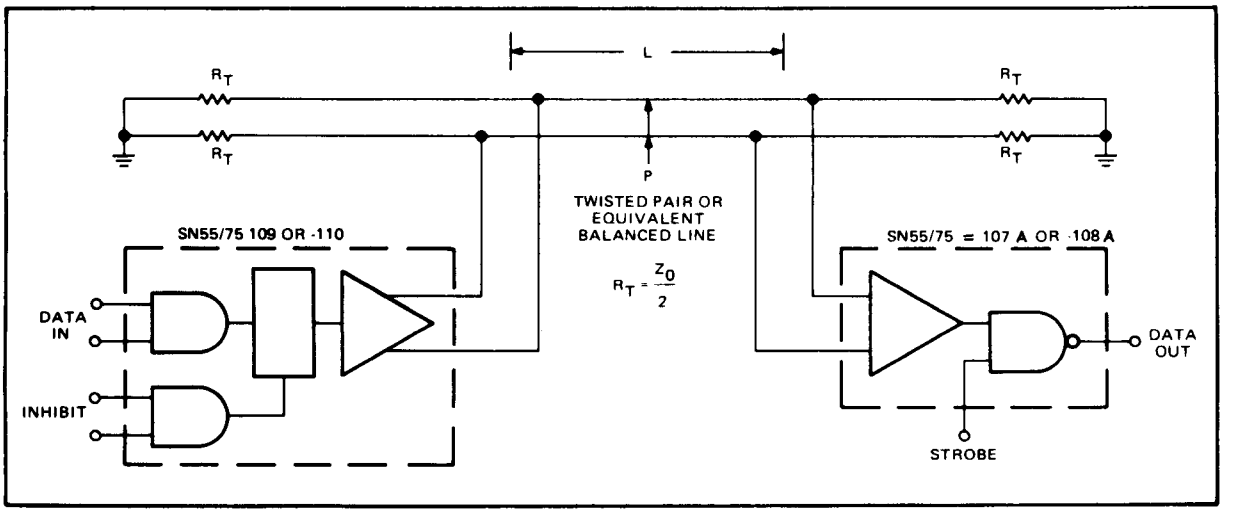


Figure 1.

USE OF SN75107 SERIES DEVICES IN A TYPICAL SINGLE-DRIVER, SINGLE-RECEIVER TRANSMISSION SYSTEM

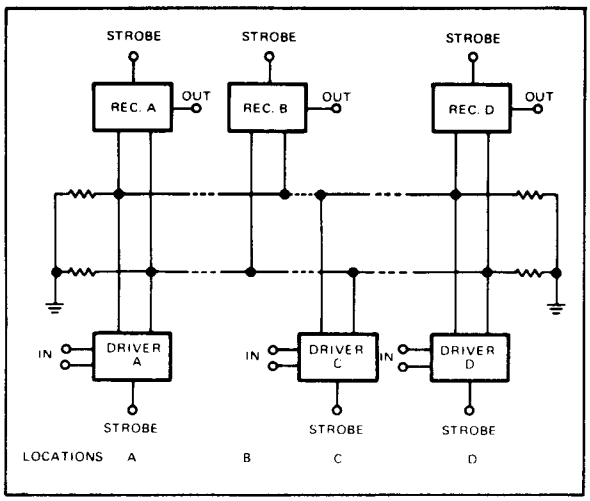


Figure 2. SIMPLE PARTY LINE SYSTEM WITH DRIVING AND RECEIVING STATIONS SCATTERED ALONG THE LINE.

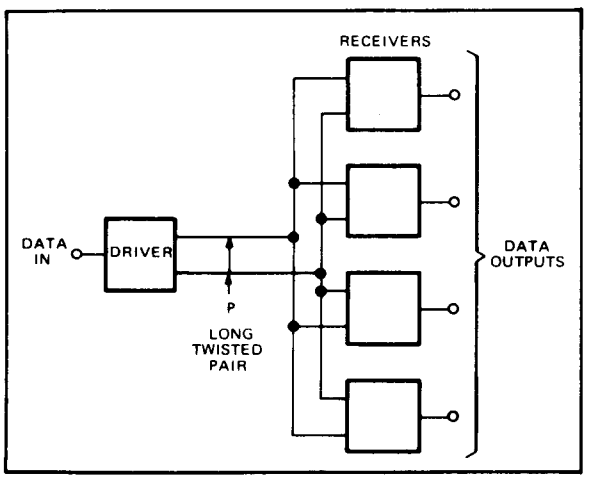


Figure 3. PARTY-LINE CONCEPT OF ONE DRIVER TRANSMITTING TO ONE OF MANY RECEIVERS

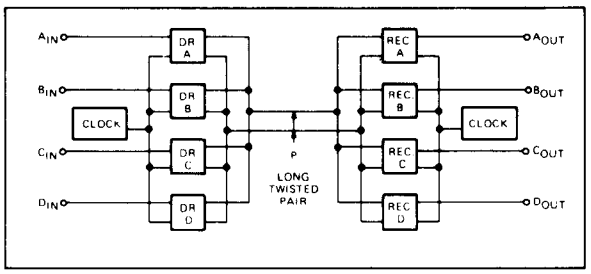


Fig. 4. CONCEPTUAL DIAGRAM OF FOUR TRANSMISSION CHANNELS SHARING THE SAME PARTY LINE

The SN75107 Series specifications allow widely-varying thermal and electrical environments at the various driver and receiver locations. The party-line system offers maximum performance at minimum cost for those applications in which it is usable.

Figure 5 shows an eight-channel party-line system similar to that in Figure 4, including clocking arrangements. This method uses two twisted pair lines: one for data transmission and the other for clocking and control information. Details of this system appear in Figures 6 and 7. Careful matching of the line delay is necessary to insure synchronized clocking. Some compensation networks might be needed.

Unbalanced or Single-Line Systems: SN75107 Series dual line circuits may also be used in unbalanced (that is, single-line) systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

In such systems, the receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal and supplying the transmission line signal to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical with respect to it for maximum noise margin. The reference voltage should be in the range of −3 V to +3 V. It can be provided either by a separate voltage source or a voltage divider from one of the available supplies.

A single-ended output from a driver is used in single-wire systems as shown in Figure 8. A coaxial line is preferred, to minimize noise and crosstalk problems. For large signals swings, the SN75110 is recommended because it has the higher output current. Two drivers may be paralleled for even higher current. The unused driver output terminal should be tied to ground as shown in the figure. The voltage at the output of the driver is then given by $V_{out} = (V_p - R2\ I_{out})\ (R1)/(R1 + R2)$, where I_{out} is the given output sinking current. The values of R1 and R2 affect the amplitude of the pulse and its position with respect to ground.

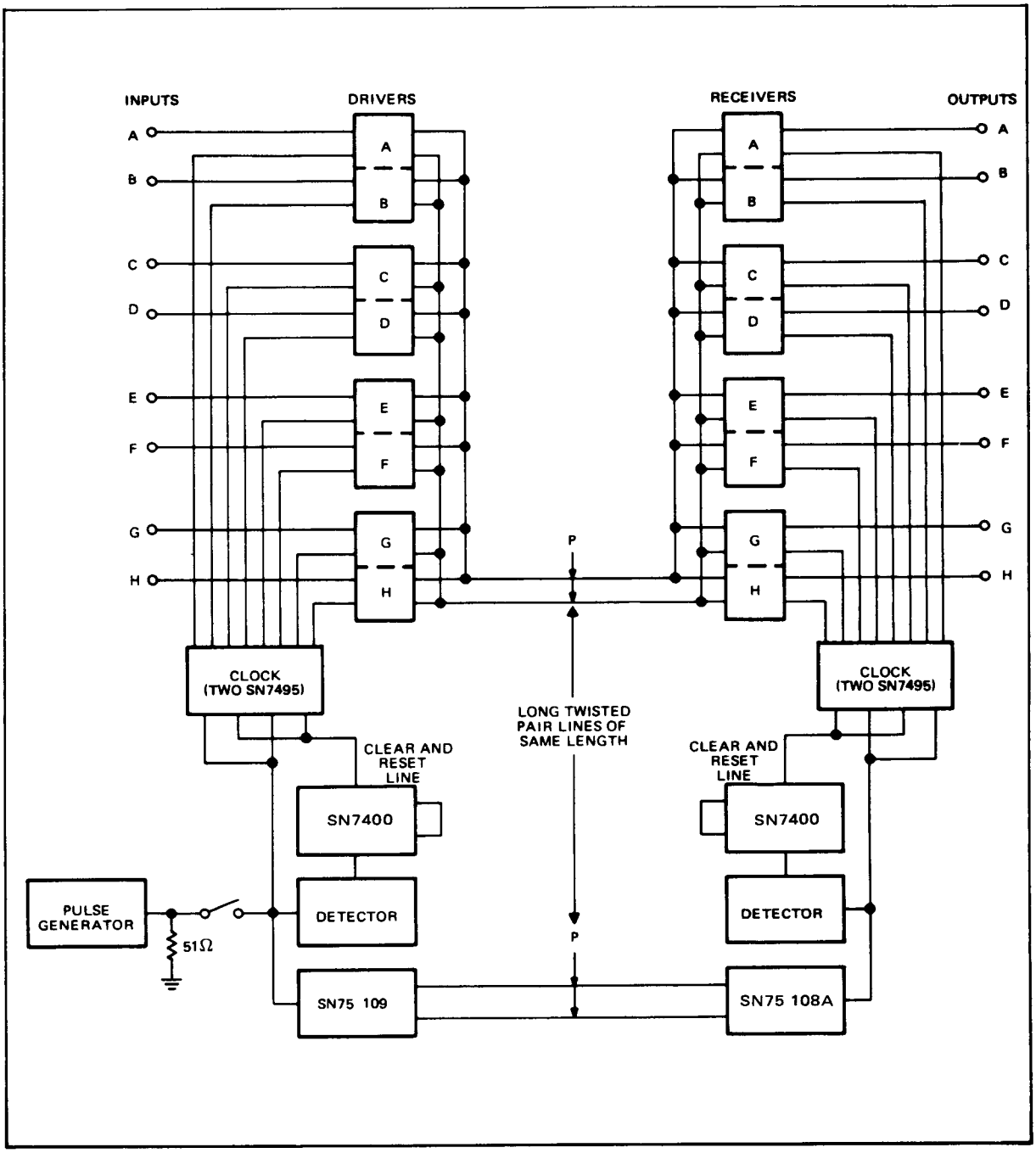


Figure 5. A MULTI-CHANNEL SYSTEM WITH CLOCKING (SEE DETAILS OF DETECTOR, CLOCK, AND TEST CIRCUIT IN FOLLOWING FIGURES)

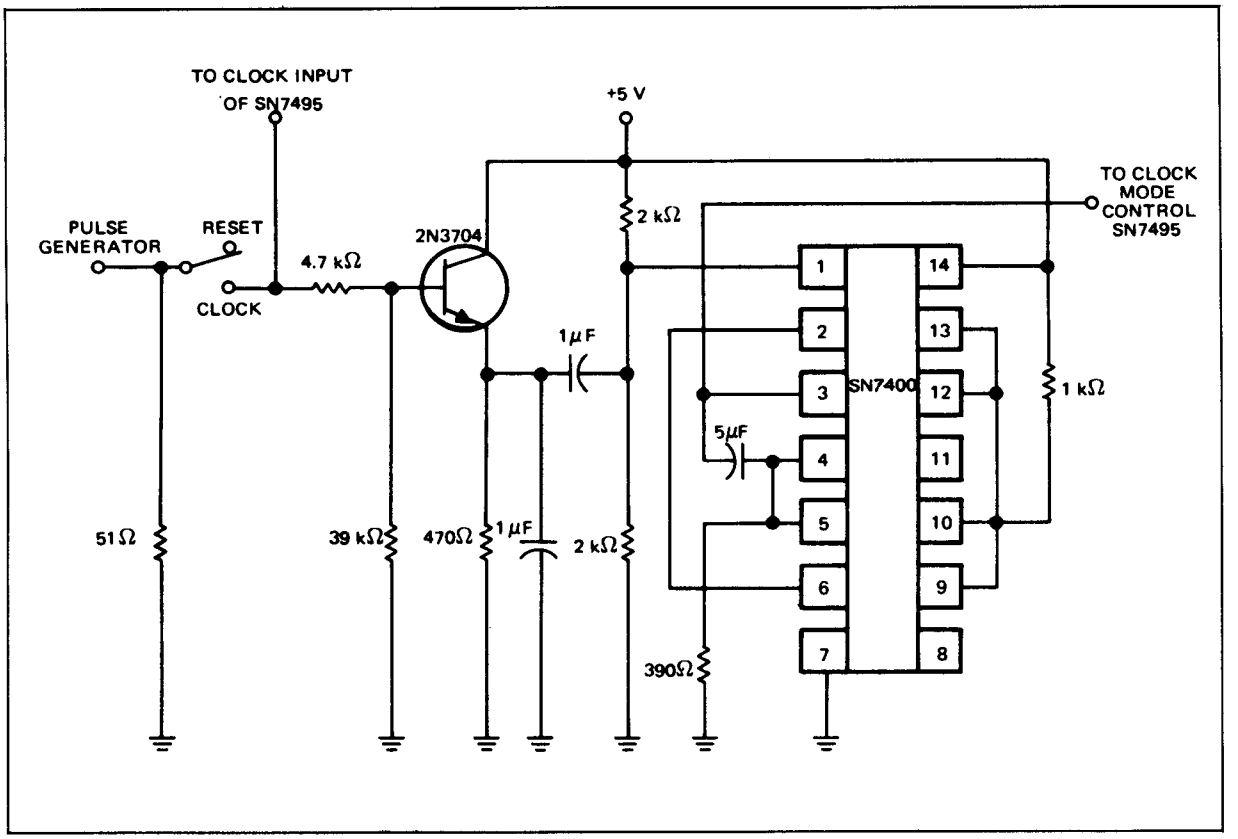


Figure 6. DETECTOR CIRCUIT FOR CLEARING SN7495 CLOCK IN Figure 5.

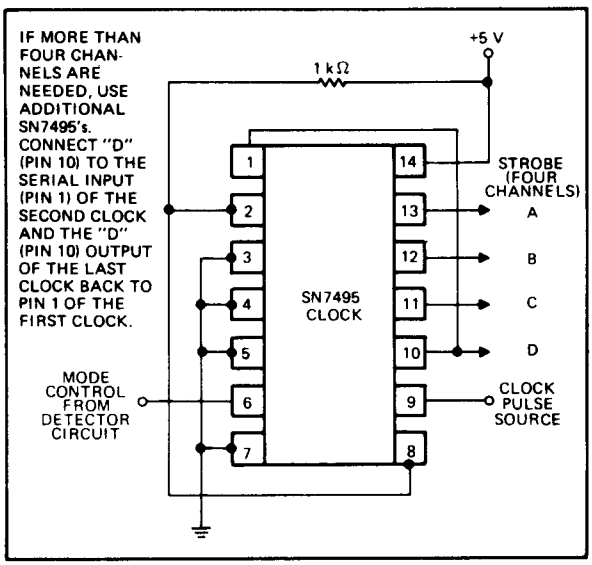


Figure 7. SN7495 CLOCK FOR STROBING DRIVERS AND RECEIVERS IN Figure 5.

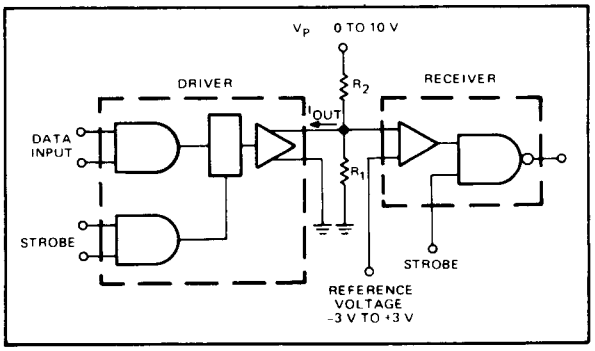


Figure 8. A TYPICAL SINGLE-LINE TRANSMISSION METHOD USING SN75107 SERIES.

APPLICATIONS OTHER THAN LINE TRANSMISSION

The possibilities of using line drivers and receivers for applications other than line driving and receiving is limited only by the ingenuity of the design engineer. The ability to go from unbalanced to balanced lines or balanced to unbalanced, to sense voltage levels, to program outputs, and other characteristics should generate many ideas for uses of these devices. Some examples are the following:

Receiver Applications:

- ECL-To-TTL Level Translators
- Dual Comparators
- Window Discriminator
- Pulse Amplitude Detectors
- Analog-To-Digital Converters
- Sense Amplifiers
- Double-Ended Limited Detectors

Driver Applications:

- TTL-To-ECL Level Translators
- Memory Pre-Drivers
- Ramp Generators
- Digital-To-Analog Converters
- MOS Digit Drivers
- Lamp Drivers

Some of these applications are outlined below.

Receiver As Dual Differential Comparator: There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt trigger, and pulse width control.

As a differential comparator, an SN75107A or-108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 9. Thus a logical "1" or "0" is

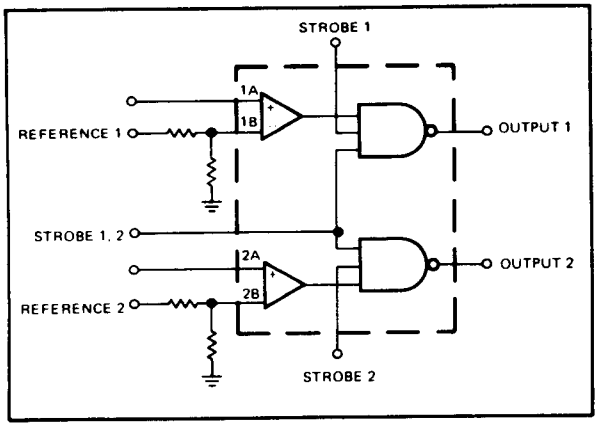


Figure 9. SN75107 SERIES RECEIVER AS A DUAL DIFFERENTIAL COMPARATOR

experienced at the output resulting from one input being greater than the other. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

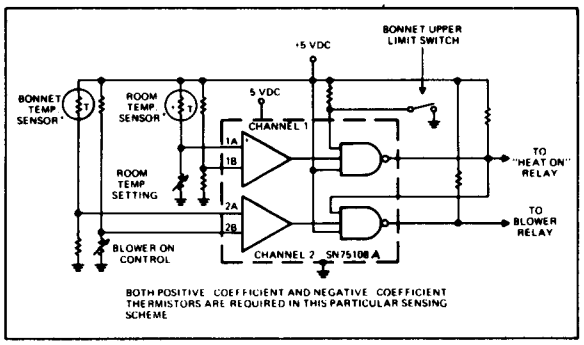


Figure 10. FURNACE CONTROL USING SN75108A

Furnace Control Using The SN/75108A: The furnace control circuit in Figure 10 is an example of the possible use of the SN75107 Series in areas other than what would normally be considered electronic systems. Basically the operation of this control is as follows. Where the room temperature is below the desired level, channel 1 noninverting input is above (more positive than) the reference level set on the input differential amplifier. This situation causes a high output, operating the "heat on" relay and turning on the heat. The output is tied to one of the strobes of channel 2, so that when channel 1 is on, channel 2 can be turned on. The channel 2 noninverting input is turned on when the bonnet temperature of the furnace reaches the desired level. Normally the furnace is shut down when the room temperature reaches the desired level and channel 1 is turned off. There is also a safety switch in the bonnet which shuts the furnace down if the temperature here exceeds desired limitations. The types of temperature sensing devices and bias resistor values used are determined by the particular operating conditions encountered.

Repeaters For Long Lines: In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a driver and a receiver as repeaters (shown in Figure 11) restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 11b. In most cases two twisted-pair lines suffice, one for the information and the other for the clock pulses.

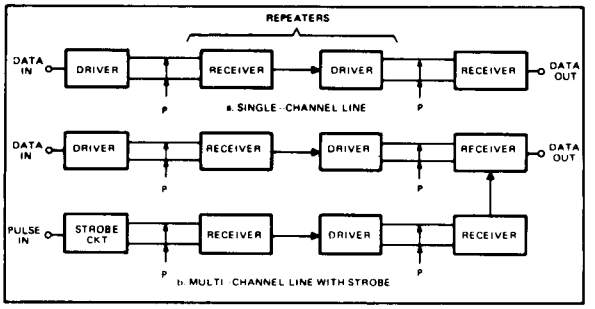


Figure 11. DRIVER-RECEIVER REPEATERS.

Window Detector: The window detector circuit in Figure 12 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time – such as detecting whether a voltage or signal has exceeded its limits or "window". A mode selector is provided for selecting the desired test. For window detecting, the upper and lower limit test position is used.

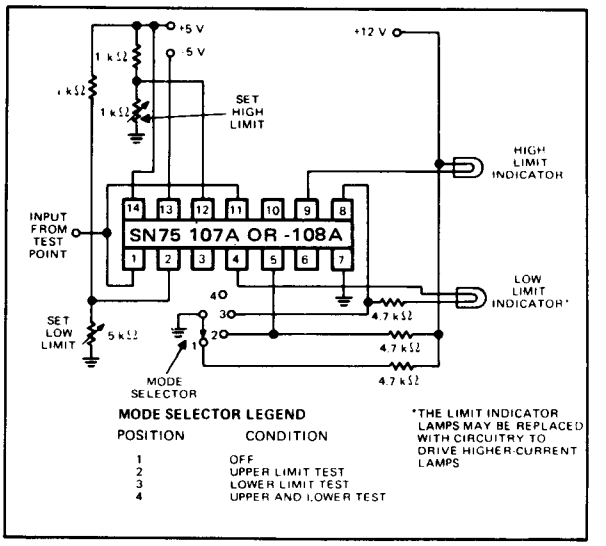


Figure 12. WINDOW DETECTOR USING SN75107A SERIES RECEIVER

Applications of SN75150 Line Driver and SN75154 Line Receiver

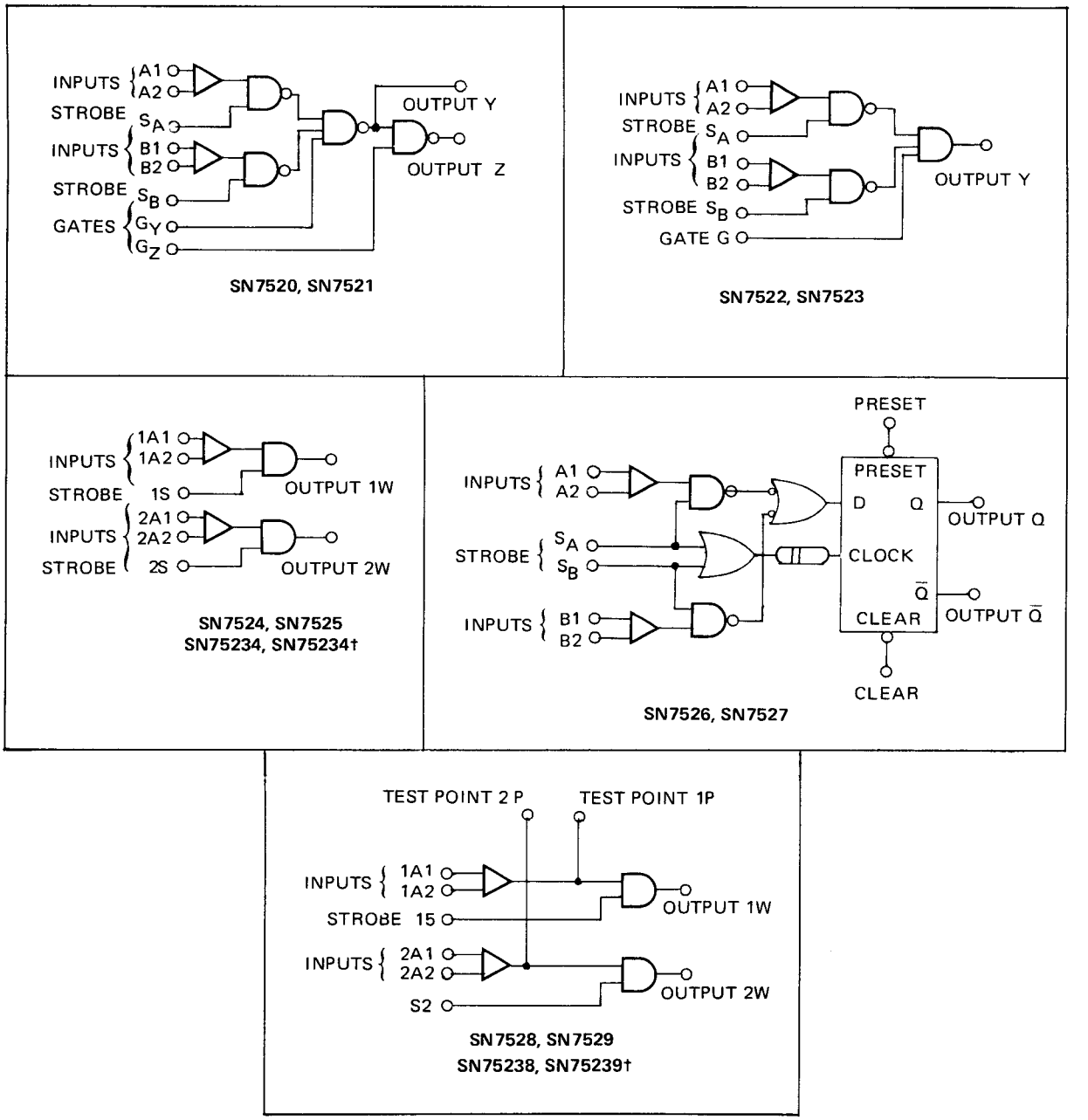
These devices have been specifically designed to meet the requirements of EIA Standard RS-232-C. They are primarily to be used, therefore, as interfaces between data terminal equipments and data communications equipment over comparatively short lengths of line, (500 feet is the maximum recommended distance), normally using coaxial line. These devices are not normally used in party-line systems, although bi-directional transmission over one line is possible as long as only uni-directional transmission occurs at any one time.

Memory Drivers and Sense Amplifiers

SENSE AMPLIFIERS

TYPE	SN7520, SN7521	SN7522, SN7523	SN7524, SN7525 SN75234, SN75235†	SN7526, SN7527	SN7528, SN7529 SN75238, SN75239†
Features	* Provide Memory Data Register * Complementary Outputs	* Open-Collector Output Stage * High Fan Out	* Dual Sense Channels * Independent Strobes	* Complete Memory Data Function * Effective Strobe Width of Less than 10 ns	* Test Points for Strobe Timing Adjustment * Dual Sense Channels
No. of Pins	16	16	16	N	N
Applications	Large Memories	Large Memories	General Purpose Sense Amplifiers	High Performance Sense Amplifiers	General Purpose Sense Amplifiers

BLOCK DIAGRAMS



† Types SN75234, SN75235, SN75238, and SN75239 are indentical to types SN7524, SN7525, SN7528, and SN7529, respectively, except that an additional stage has been added to the output gate to provide an inverted output.

MEMORY DRIVERS

TYPE	SN75324 DRIVER WITH DECODE INPUTS	SN75325 DRIVER WITH DECODE INPUT
Features	* Four 400-mA Transistors * TTL-Compatible Inputs * Internal Decoding and Timing Gates * Single 14 V Supply	* Four 600-mA Transistors * TTL-Compatible Inputs * Internal Decoding * 5 V Supply * 24 V Output Capability
Application	* Core Memories	* Core Memories * Plated-Wire Memories * Hammer Driver
No. of Pins	14	16

General Considerations

Sense Amplifiers

1. Power supplies should be regulated to ±5% or better and should have low-inductance by-pass capacitors as physically close as possible to each sense amplifier.
2. The data input/sense line should be terminated in its Characteristic Impedance and should be as short as possible. It should be kept as far away as possible from any lines carrying high level logic signals.
3. If the input signal from the momory does not have a high enough slew-rate the output of the sense amplifier may oscillate.
4. Strobe inputs to unused channels should be grounded, failure to do this may cause a malfunction inthe used channel, due to unused channels switching on noise signals. Care should be taken in the timing of the strobe signals, allowing for the propagation delay through the device.

Memory Drivers

5. Circuit-board mounting of memory drivers should be carefully considered, with special regard for heat sinking, signal transmission, and noise. Furthermore, because memory drive and logic currents may share the same electrical ground in a direct-coupled system, special care is necessary to minimise ground noise. In the case of the SN75324 this is especially so because the logic and driver are monolithic.

Application of Series SN7520 Sense Amplifiers

General

Series 7520 sense amplifiers are designed specifically for use in coincident current memories organized in the 3D (three dimensional) and 2 1/2D configurations. In these applications, memory output information is transformed from low-level (10-60mV) bipolar pulses into high-level digital logic levels. Memory information is categorized as representing stored logical "0" or "1" information on the basis of signal amplitude and position in time, regardless of signal polarity.

In these memories, it is common practice to limit the number of cores on each sense line to about 4K. Large core planes are sectored into small sub-planes of approximately 4K bits as shown in Figure 1 with separate sense lines for each sub-plane.

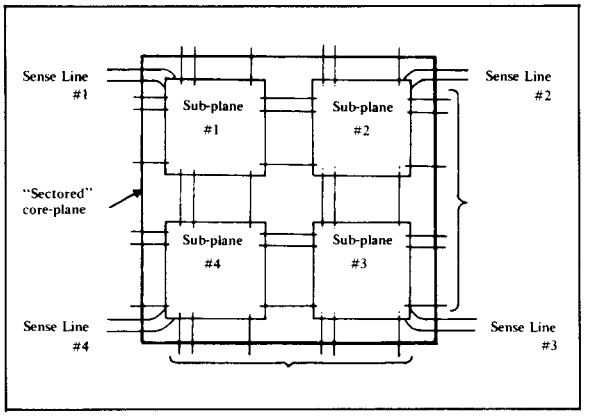


Figure 1.

Discrete sense amplifier designs usually utilize reactive components such as inductors and capacitors to eliminate problems due to d.c. bias level drift. Integrated sense amplifiers usually use capacitive coupling for the same reason. Or, a d.c. comparator is used with a complicated input resistor network to obtain threshold action. These methods, however, introduce additional problems:

(1) Reactive coupling usually results in threshold shift with increased repetition rates
(2) Reactive coupling results in excessive overload recovery time
(3) Input resistor networks degrade the common-mode rejection of the design and require expensive, precision components.
(4) Redundant circuitry results in excessive power
(5) High package or component count uses excessive board area, excessive interconnections, and reduces reliability.

Series 7520 devices incorporate the necessary circuitry to perform sensing for two sense lines without the above undesirable characteristics. This performance results from the unique Series 7520 "matched-amplifier" circuit design which utilizes the inherent matching and tracking characteristics of integrated circuit components. This design permits an all d.c.-coupled circuit without the associated d.c. drift problems. The result is close matching of all the sense channels for maximum system performance.

This results in a much higher signal-to-noise ratio than can be obtained with a larger number of cores on a sense line. Also, delays from various bit locations are more uniform, allowing more precise strobing.

The following sections show some of the applications for which the Series 7520 devices were designed.

SN7520/21N Applications

The SN7520/21N Sense Amplifier is a complete monolithic sub-system incorporating all the necessary threshold, strobing, and logic functions for sensing, gating, and storing information from up to 8K cores in the memory. The output circuit of the SN7520/21N is composed of two cascaded NAND gates. External inputs are available as logic inputs to each of the gates. The gates may be connected in a cross-coupled gate latch configuration, ($\overline{Q}$ output to Gate Q input), as shown in Figure 2, thus enabling the output circuit to function as part of the Memory Data Register (MDR). Information extracted from the sense lines during the strobe enable pulse can be retained as long as desirable for use with the computer logic section. A negative going pulse applied to the Gate Q input clears the latch prior to the next strobe enable pulse.

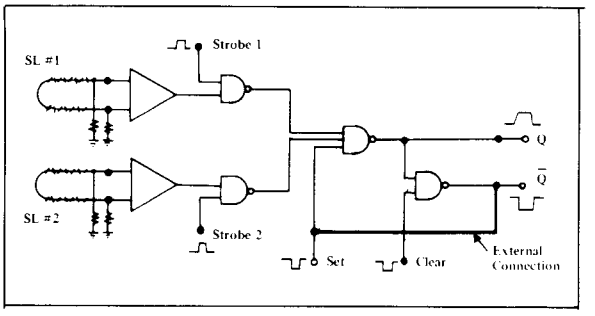


Figure 2.

In those applications where output pulse stretching is desirable, the gates in the output section of the SN7520/21N may be capacitively coupled, as shown in Figure 3.

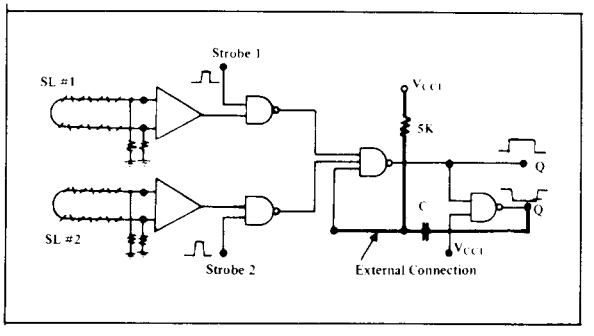


Figure 3.

In some applications, neither the latch configuration or output pulse stretching may be required. In these applications, the gates in the output of the SN7520/21N may be used as a part of the logic unit, supplying complementary output logic levels with standard TTL fan-out capability.

In applications that do not utilize the external gate inputs (Gate Q and Gate $\overline{Q}$ inputs) these terminals should be tied to the positive supply (Vcc_1) to prevent capacity coupling at these terminals from affecting delay times. Strobe inputs should be treated similarly.

In some memory applications, more than 8K words may require sensing. The dual sense input function of the SN7520/21N may be expanded to four sense inputs by the addition of a dual-input SN7522/23N sense amplifier. (The 4K bits per sense line referred to in this report is a good rule of thumb, resulting in a good signal-to-noise ratio, thereby permitting good system performance. However, in especially clean (low noise) memory designs, it may be possible to have 8K or more bits per sense line). Details in using the SN7522/23N as an expander will be considered in detail in the next section.

SN7522/23N Applications

The SN7522/23N has as its output circuit an open-collector gate that may be connected to perform the Wire-OR logic function, thus permitting a level of logic to be implemented without additional gate delays. Each SN7522/23N also has an internal load resistor of value approximately 2KΩ. One end of the resistor is internally connected to the positive supply (Vcc_1) while the remaining end is brought out through a separate pin. The resistor may be used as a collector pull-up resistor in those applications where its value is acceptable. Load resistors from several SN7522/23N packages may be connected in parallel for lower impedance.

The output gate of the SN7522/23N is designed to have a very high sink current capability. Although the specifications indicate a limit of 0.4 volts maximum output logical 0 voltage level while sinking 16 milliamps, this limit is conservative as indicated by the typical curve for this parameter, shown in the data sheet.

The high output sink current capability increases the versatility of the SN7522/23N in a variety of applications. Several SN7522/23Ns may be Wire-OR connected in order to provide the necessary number of sense-inputs for large memory applications. Also, the output may be Wire-OR connected with other sense amplifiers such as the SN7520/21N. In this application, shown in Figure 4, the output of a single SN7520/21N is connected as a latch to function as

part of the Memory Data Register. As many SN7522/23Ns as necessary are connected to provide additional sense inputs to the MDR. The Gate Input terminal of each of the SN7522/23Ns, in this application, serves as an external set input for the MDR, allowing information to be entered into the MDR from the logic section. The Gate $\overline{Q}$ input of the SN7520/21N serves as the Clear input for the latch in this application.

The output of the SN7522&23N may also be Wire-OR connected with logic gates that feature this capability. This includes most diode-transistor logic (DTL) gates and the Series 74, SN7401N, quad two-input positive NAND gate.

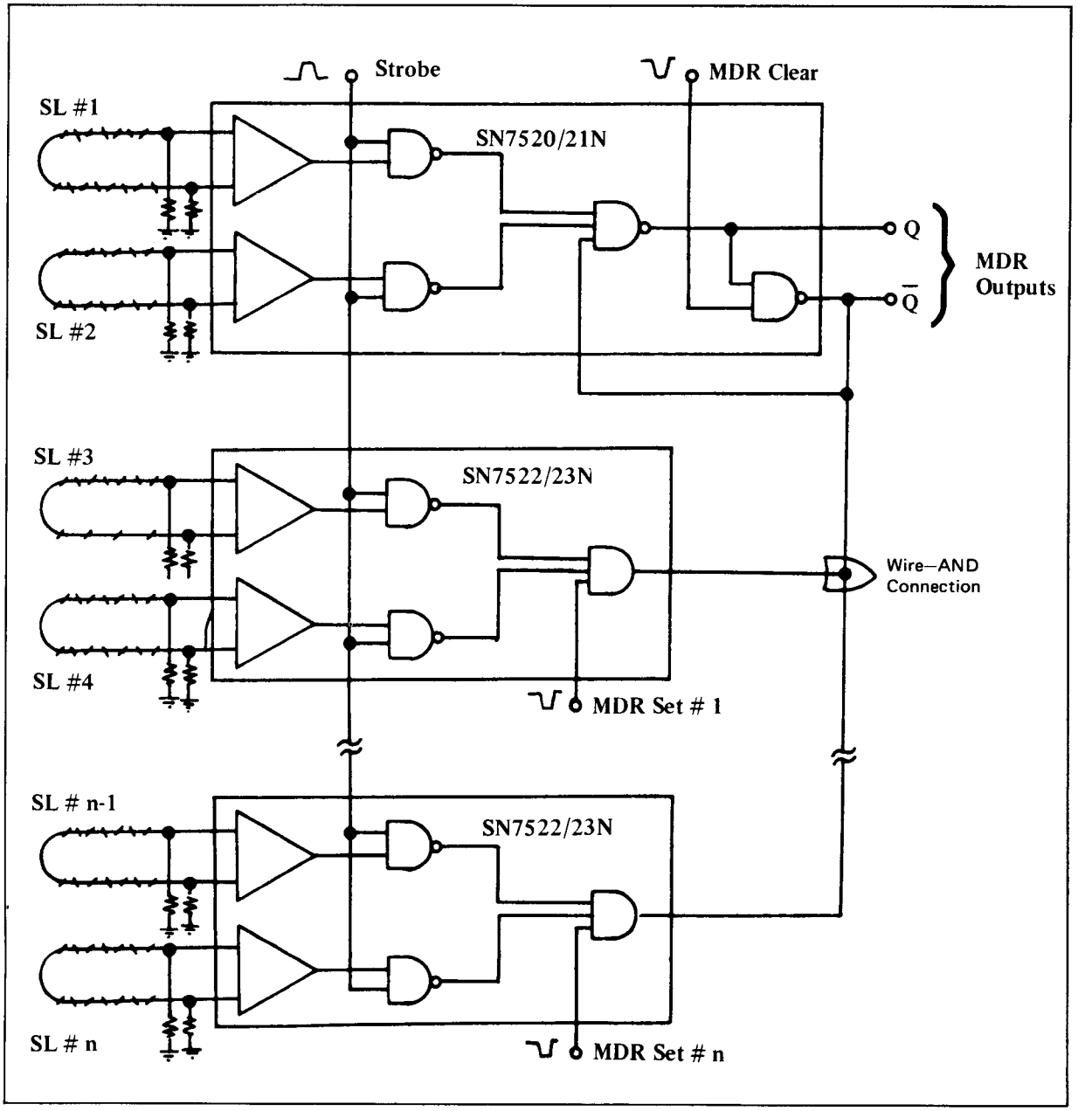


Figure 4. USE OF THE SN7522/23N AS AN INPUT EXPANDER FOR THE SN7520/2IN

In applications in which more than a simple latch is desirable for the MDR, several options may be considered. For example, the SN7474N dual D-type edge-triggered flip-flop is an excellent device for use with the SN7522/23N. The SN7474N features direct clear and preset inputs and complementary outputs. Input at the D input is transferred to the Q output of the SN7474N on the positive edge of the clock pulse. The outputs of one or more SN7522/23Ns can be connected as shown in Figure 5 to provide inputs to the SN7474N.

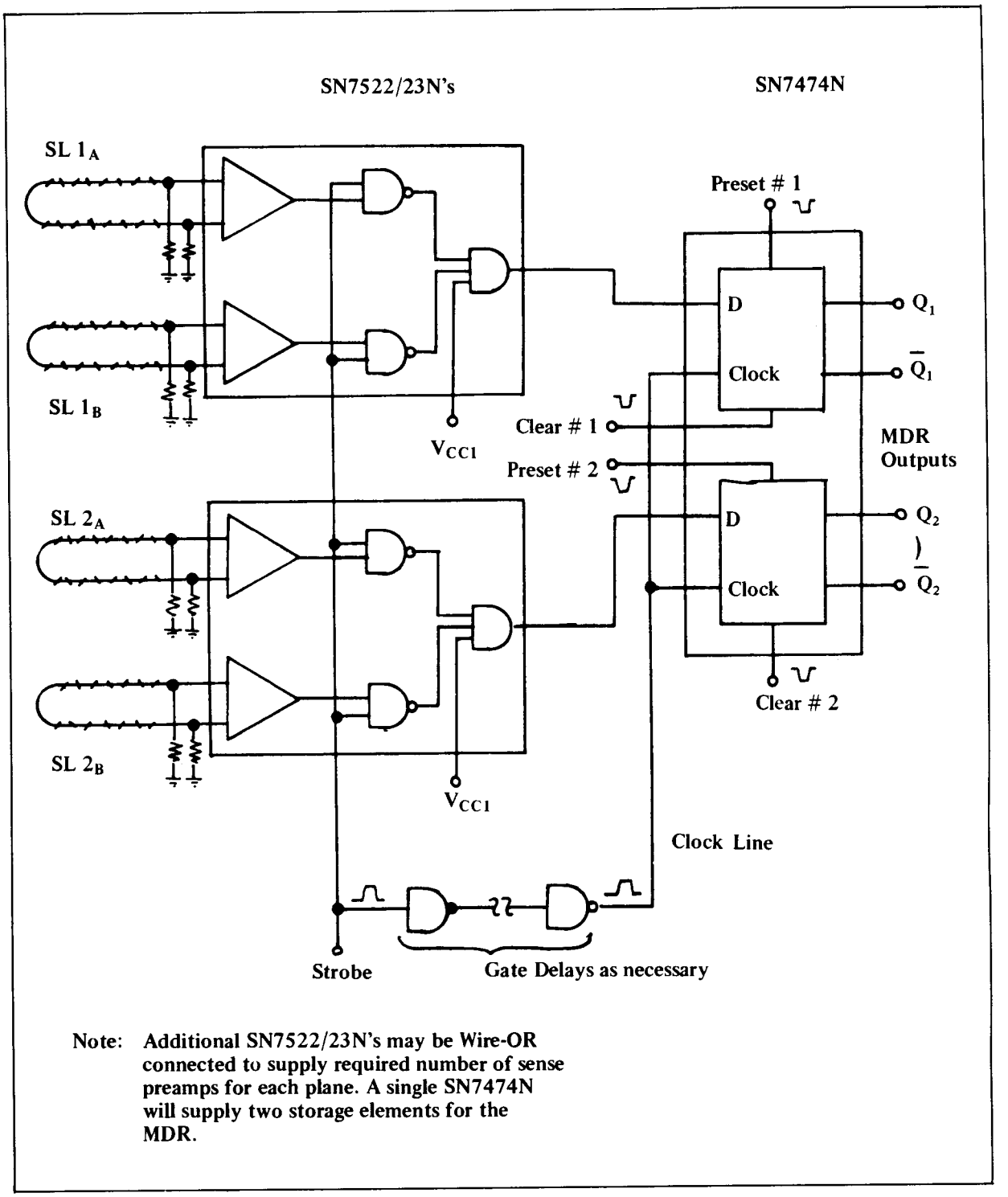


Figure 5. USE OF SN7522/23N WITH SN7474N AS MEMORY DATA REGISTER

A single SN7474N can provide two storage elements for the MDR. If a separate clock pulse is undesirable, the clocking function can be provided by the strobe input. Proper delay must be provided to ensure that the D input is set-up at clock time. In this application, an inversion occurs from the sense inputs to the flip-flop output. Logical 1 sense inputs ($> V_T$) will enter logical 0 levels into the Q output. This is due to the negative-goining output from the SN7522/23N.

SN7524/25N Applications

The SN7524/25N sense amplifier is, in actuality, two separate sense amplifiers in a single package. Separate inputs, strobes, and outputs permit a single SN7524/25N package to service two separate bit-planes in a memory as shown in Figure 6. Since the outputs of the SN7524/25N cannot be Wire-OR connected because of its normally-low output level, the SN7524/25N finds its widest application in small memories of up to about 4K words. In this application, the SN7524/25N will result in one-half the package count normally required. It also increases reliability and reduces the memory size by fewer interconnections, less board area, and less power than other sensing schemes.

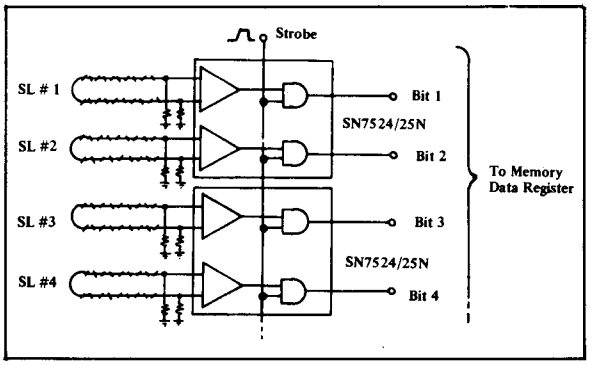


Figure 6.

A useful application of the SN7524/25N is in conjunction with the SN7475N quadruple bistable latch, as shown in Figure 7.

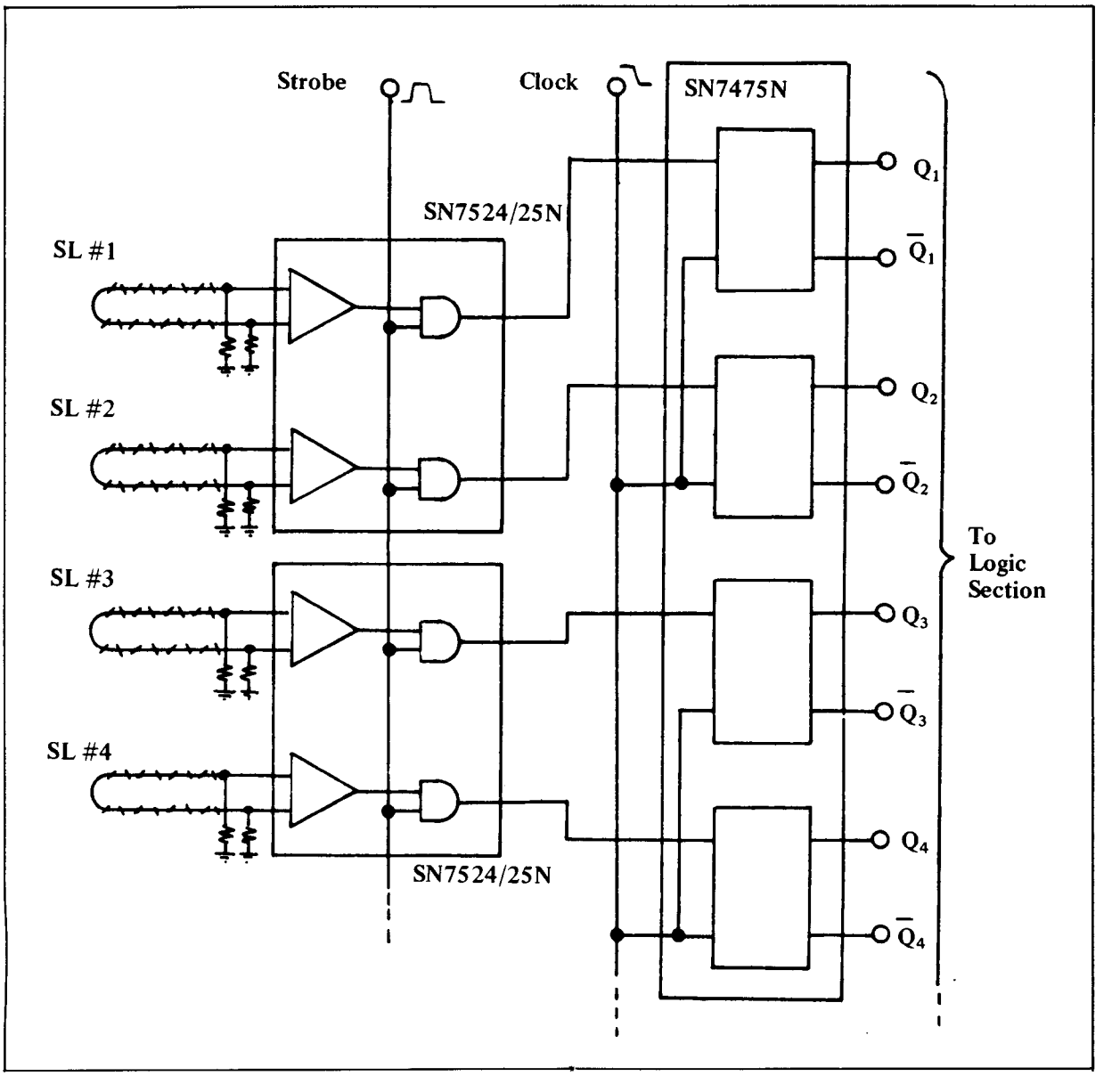


Figure 7.

In this application, the SN7475N functions as the memory data register (MDR) for two of the SN7524/25N packages. Four bits of the memory word can thus be sensed and stored with only three integrated circuit packages. Operation can be explained as follows. As long as the clock input to the SN7475N is high, the Q output follows the D input. When the clock input goes low, the information contained in the latch is retained until the clock input is permitted to return to the high state. When used with the SN7534/25Ns the SN7475N can be used to retain information read from the memory for as long as is desirable. The negative edge of the clock must be timed so that it occurs while the desired information is present at the output of the SN7524/25N sense amplifiers.

For a more exotic application, a SN7474N dual d-type flip-flop may be used with a SN7524/25N in Figure 8.

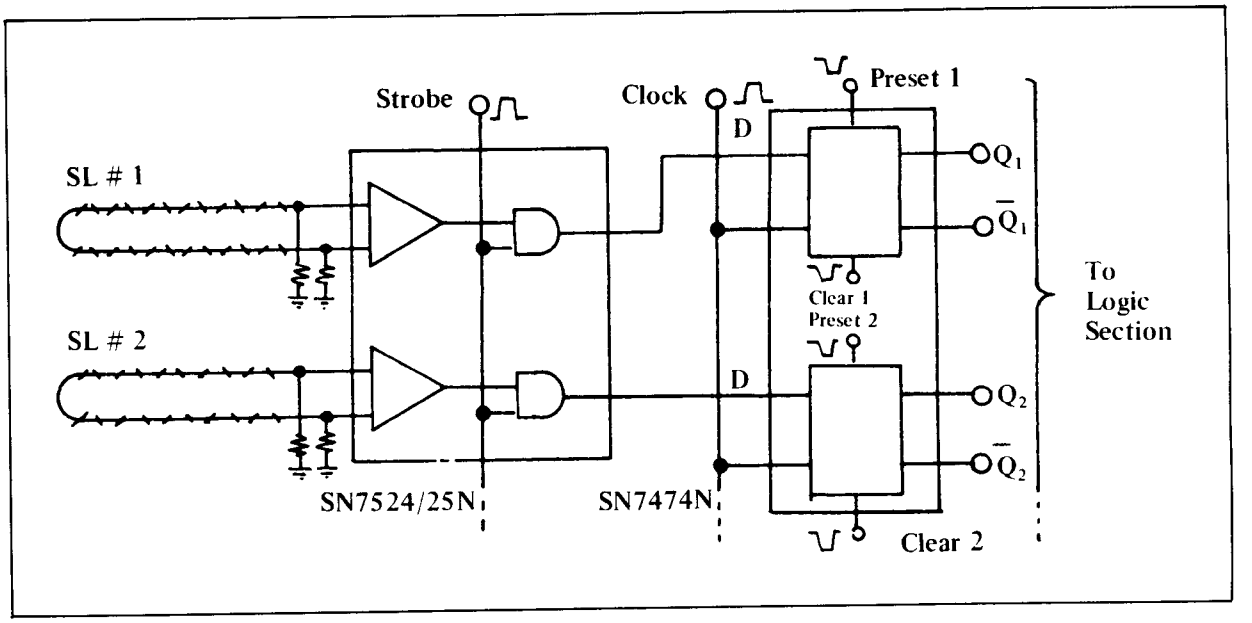


Figure 8. THE SN7474N FUNCTIONS IN A MANNER SIMILAR TO THE SN7475N

The SN7474N functions in a manner similar to the SN7475N. Operation is as follows. The positive edge of the clock pulse shifts the information present at the D input to the Q output of the flip-flop. The Q output does not "follow" the D input except in the clock pulse command. The strobe input pulse may be used to supply the clock input pulse by adding the proper delays, see Figure 9.

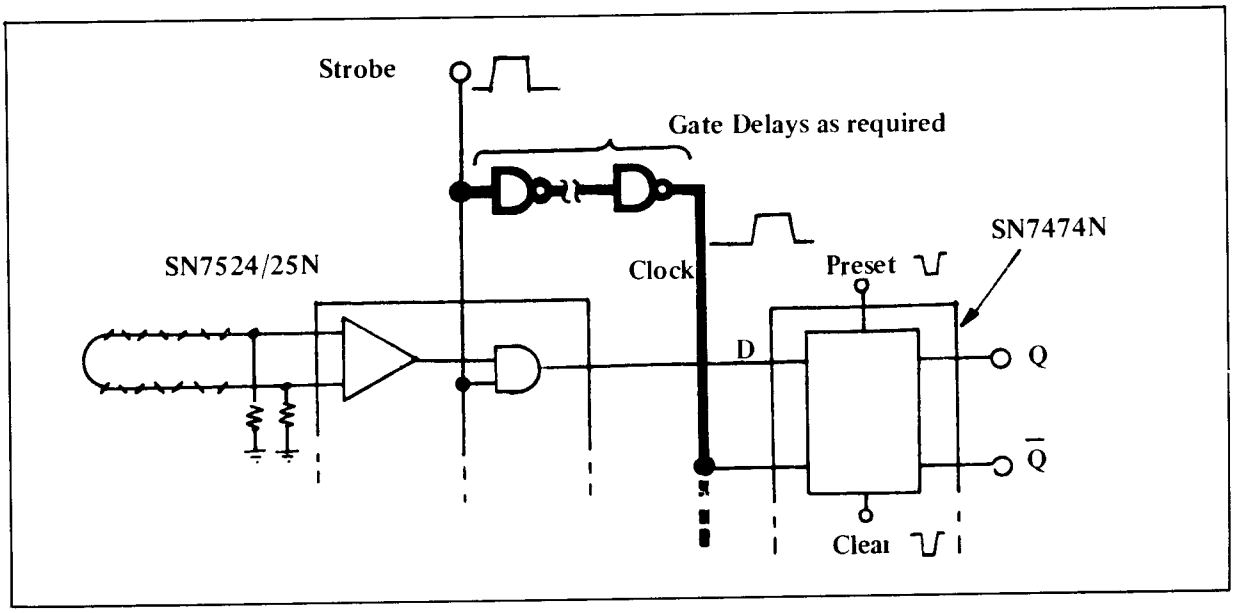


Figure 9.

The positive edge of the strobe pulse should occur during the input pulse. The delays introduced from the strobe input to the clock input will allow the sense information to propagate to the D input of the flip-flop, thereby insuring that the clock pulse is properly timed with respect to the D input information. Since each SN7474N contains two D-type flip-flops two planes can be serviced by a single SN7474N and a single SN7524/25N. The SN7474N may be desirable over the SN7475N since it includes external set and clear inputs, allowing entry into the two bits of the memory data register (formed by the SN7474N) from an external source.

If it becomes desirable to "OR" the outputs of the SN7524/25N, this can readily be accomplished with the addition of a positive NOR gate, such as is a part of the SN7402N TTL device, as shown in Figure 10. This device is a quadruple 2-input positive NOR gate.

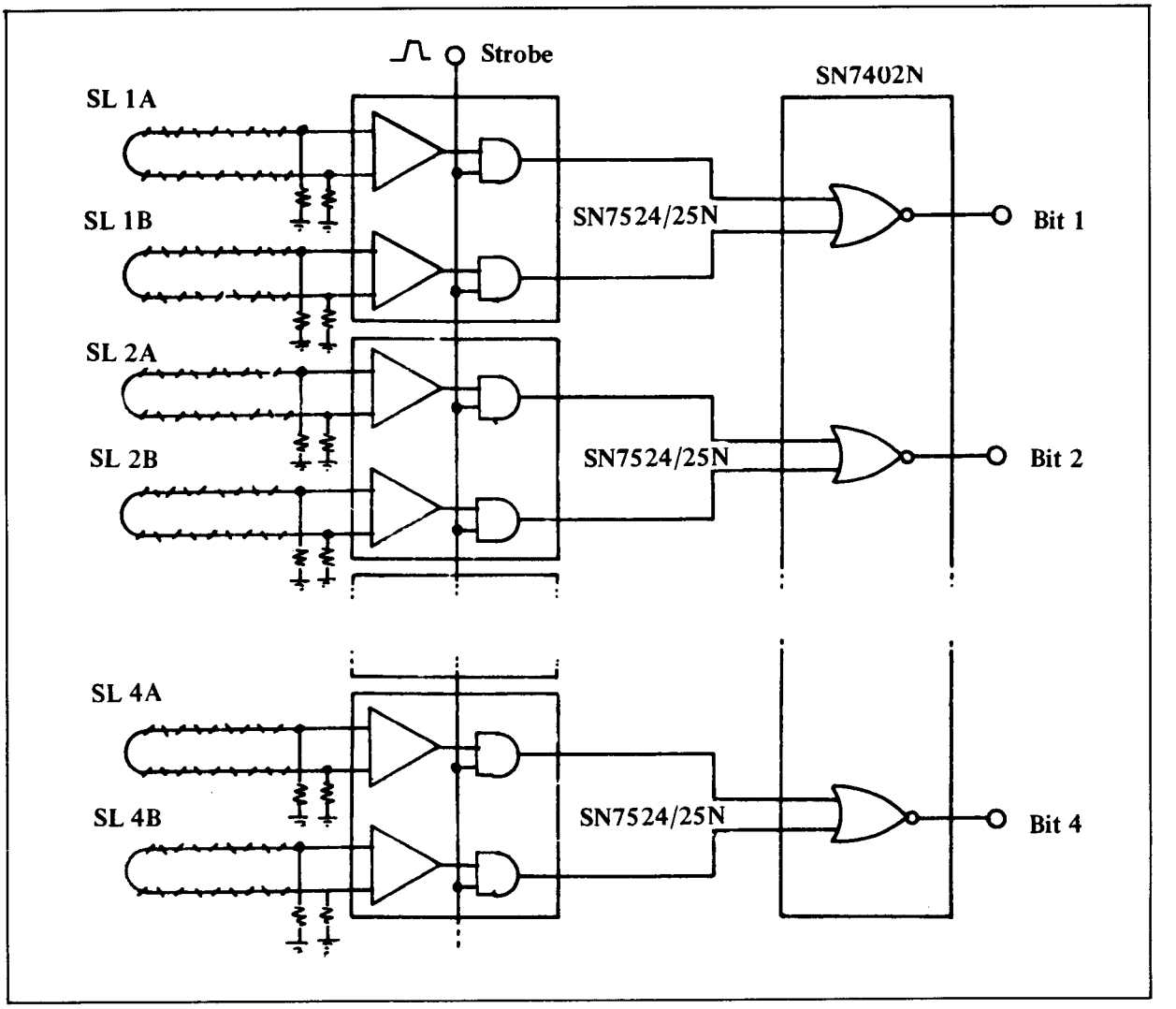


Figure 10.

The SN7402N can "OR" four pairs of SN7524/25N outputs. If more than two outputs are desired in the OR connection, it is more desirable to utilize the Wire-OR capability of the SN7522/23N in this application.

Typical System Applications

The following figures (Figures 11 to 14), show in detail how the Series 7520 sense amplifiers can be used in either 3D or 2 1/2D memory applications. These are representative memories and may not apply to all memory configurations of the 3D or 2 1/2D type. However, the basic sense amplifier application can be seen.

In either application, the most optimum threshold level can be determined for the memory by adjusting the threshold levels of the sense amplifiers. In extremely "tight" designs, it may be desirable to adjust sense amplifier threshold levels on an individual package basis. On less stringent applications, all threshold levels may be adjusted in parallel.

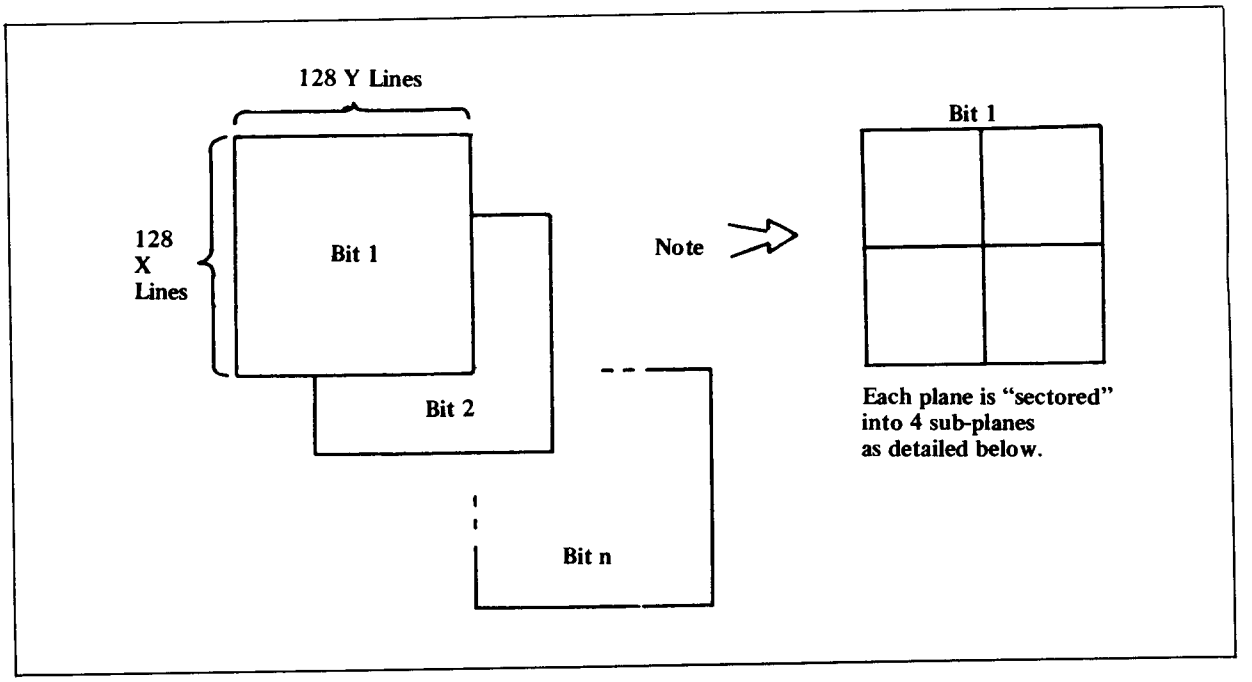


Figure 11a. LOGICAL MEMORY ORGANIZATION

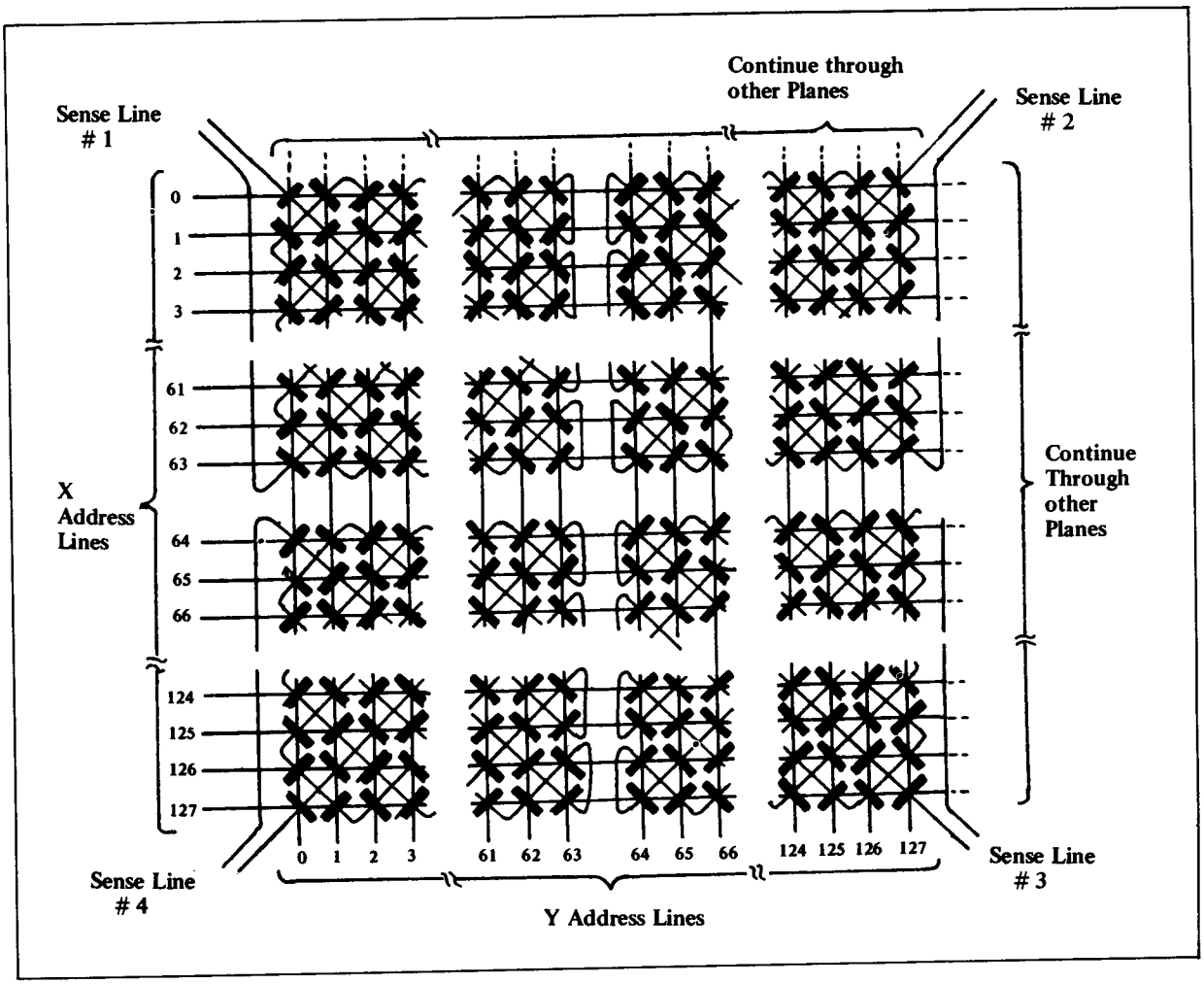


Figure 11b. DETAILED MEMORY WIRING

Figure 11. TYPICAL 3D MEMORY APPLICATION (16K N-BIT WORDS)

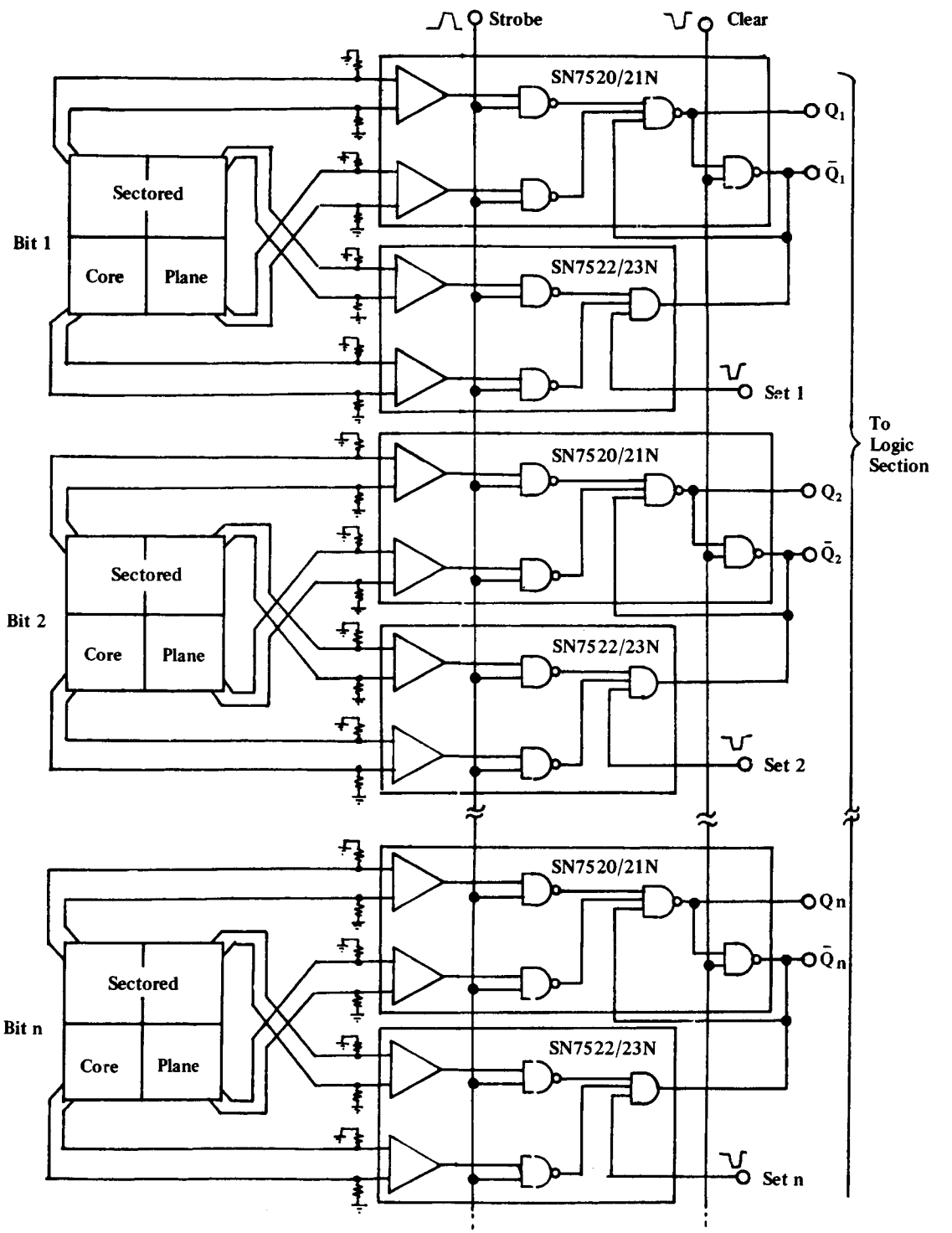


Figure 12. USE OF SN7520/21N AND SN7522/23N WITH 16K WORD 3D MEMORIES

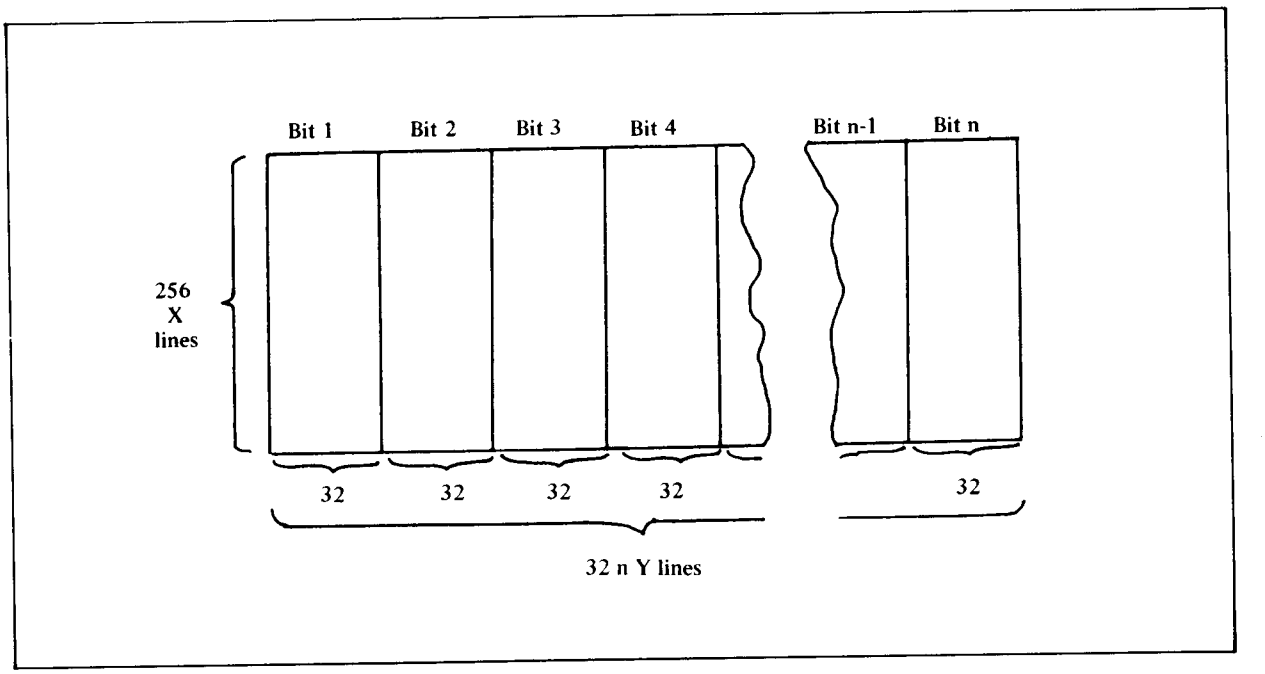


Figure 13a. TYPICAL LOGICAL MEMORY ORGANIZATION

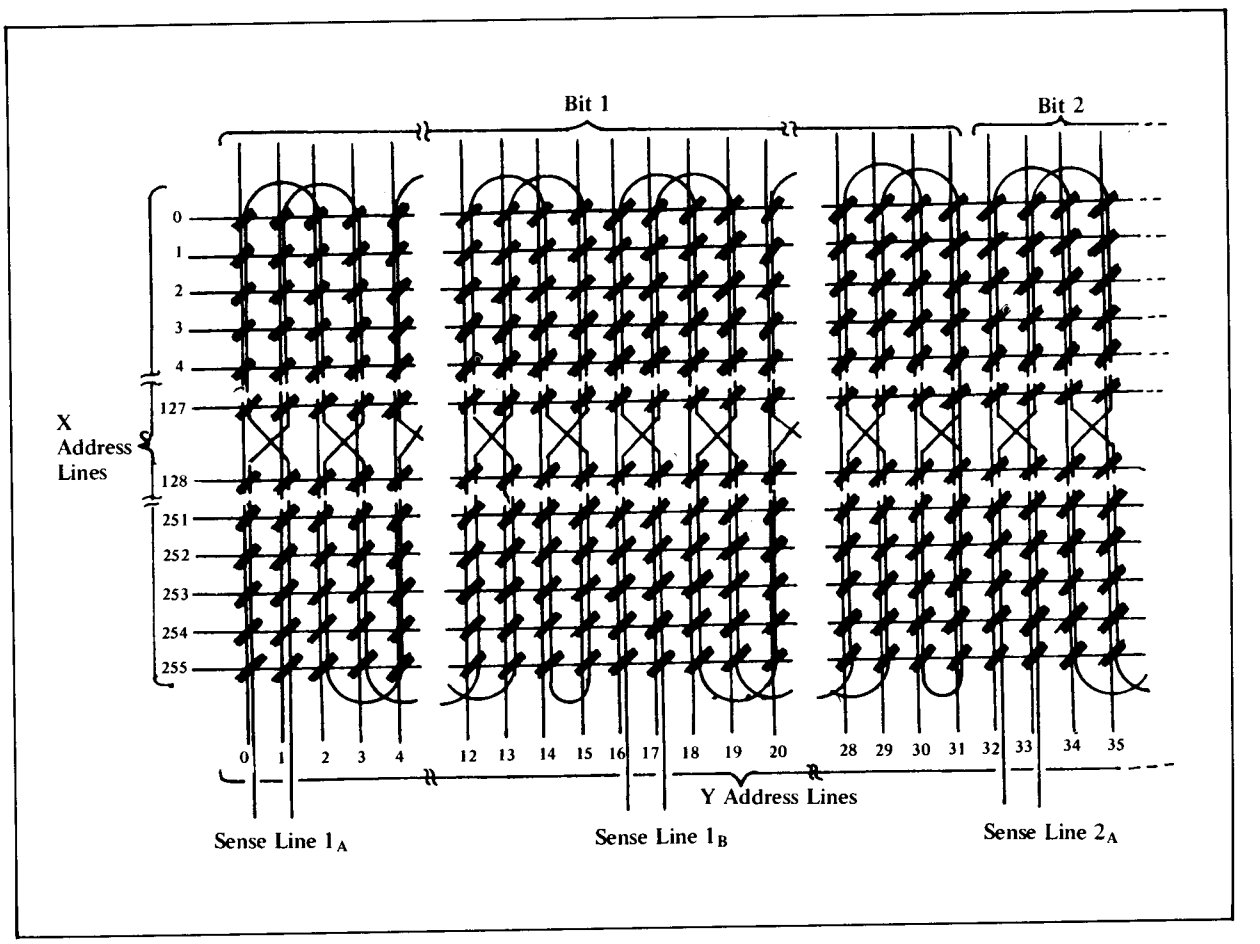


Figure 13b. DETAILED MEMORY WIRING

Figure 13. TYPICAL 2 1/2D MEMORY APPLICATION (8K N-BIT WORDS)

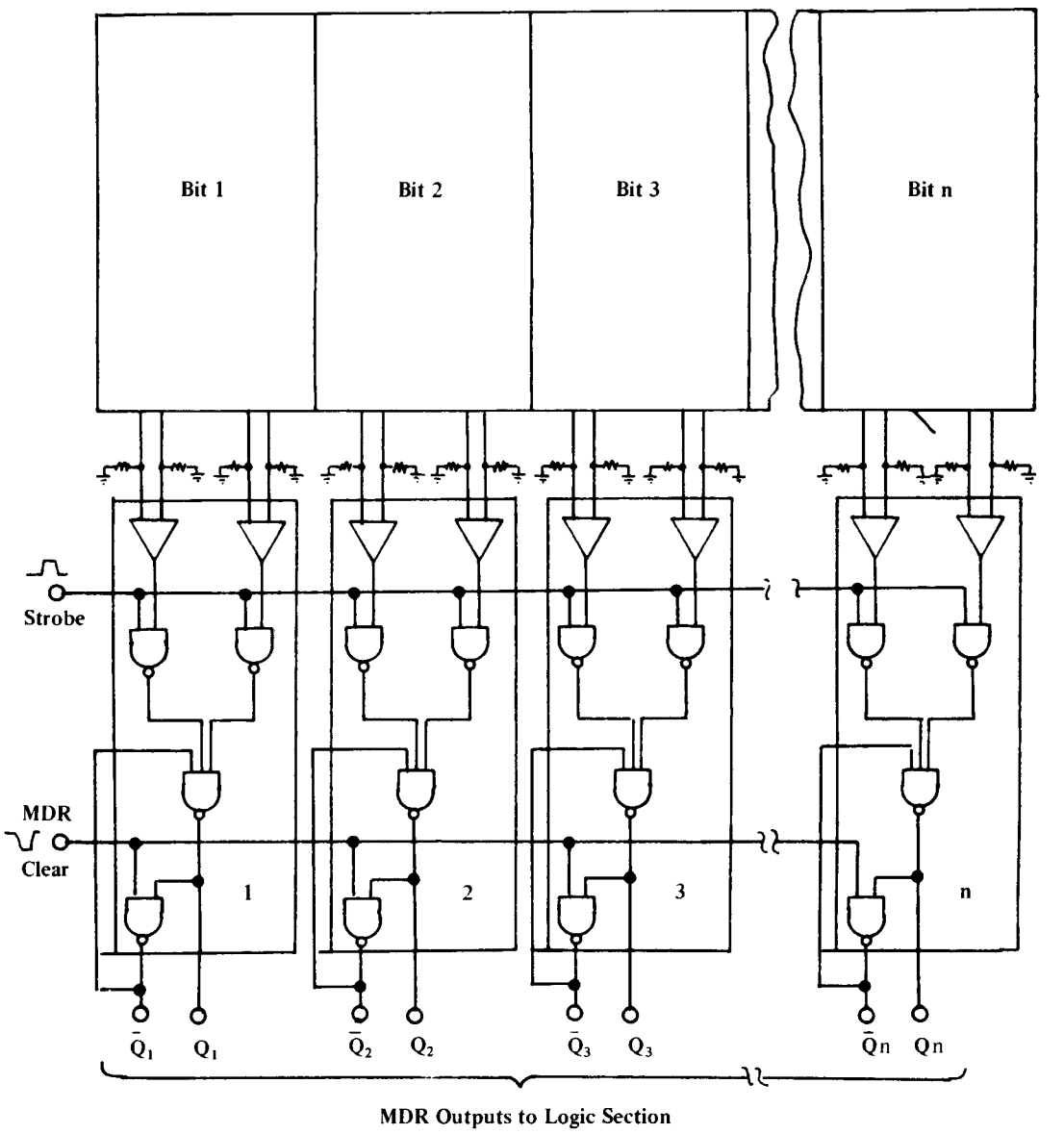


Figure 14. USE OF SN7520/21N WITH 8K WORD 2 1/2D MEMORY (SN 7520/21N CONNECTED IN MDR LATCH CONFIGURATION)

Applications of the SN75324 Monolithic Memory Driver

This section briefly describes the SN75324 monolithic integrated-circuit memory driver and illustrates how to use it to address and drive a magnetic memory. Detailed specifications of this circuit are found in the appropriate data sheet.

Description of SN75324

A functional diagram of the SN75324 appears in Figure 1. This unit is designed specifically to replace

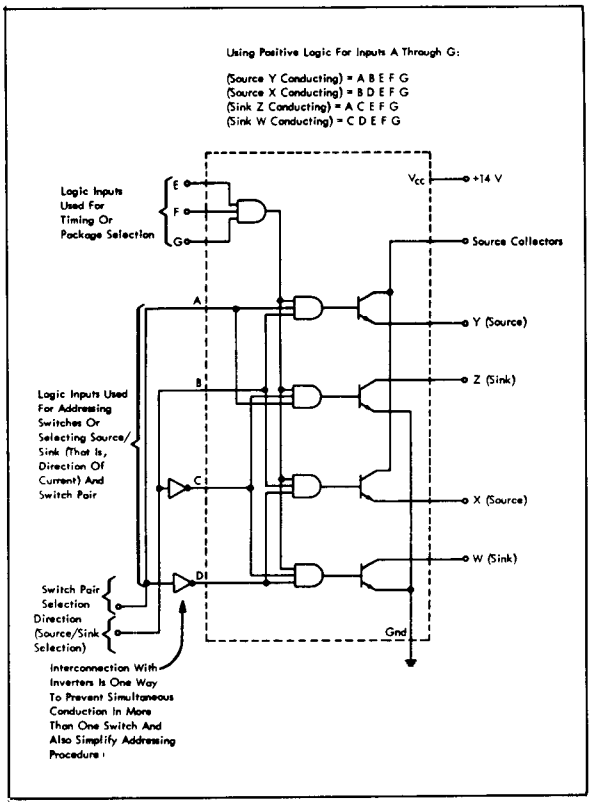


Figure 1. SIMPLIFIED FUNCTIONAL DIAGRAM AND LOGIC TABLE FOR SN75 324 WITH TYPICAL INTER-CONNECTION OF ADDRESS INPUTS

traditional discrete transistor-transformer circuits in magnetic memory systems. However, it can also be used as a lamp driver, relay driver, or high-fan-out logic gate. It consists of four fast, high-current switches controlled by seven logic inputs (denoted A through G) that are compatible with 74 TTL and other standard logic systems with precautions mentioned under "Logic Input" below. One pole of each switch leads outside the unit (outputs W,X,Y, and Z). On their opposite poles, two of the switches connect to the memory current source, and the other two connect to ground. Thus two outputs are sources and two are sinks for memory drive current.

The decoding circuitry is arranged so that any or all of the switches in a package may be conducting at any given time. However, the unit will overheat if more than one switch at a time carries memory current. Therefore the system must be designed to prevent this occurrence by such means as the external logic inverters shown in Figure 1.

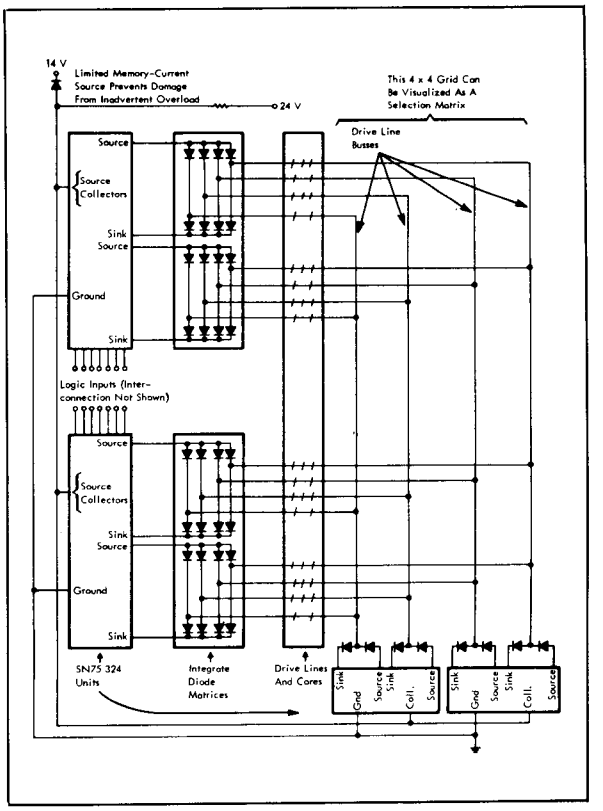


Figure 2. TYPICAL APPLICATION OF SN75324 IN MEMORY-DRIVE: A SELECTION SCHEME FOR 16 DRIVE LINES

Memory-Drive Applications

In memory-drive applications, the SN75324 can be connected in any of several fashions. Typically, however, sources and sinks are arranged in pairs from which many drive lines branch off, as shown in Figure 2. Here each drive line is served by a unique combination of two source/sink pairs, so that a selection matrix is formed. The size of such a matrix is limited only by the number of drive lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive line of the particular system imposes on the driver.

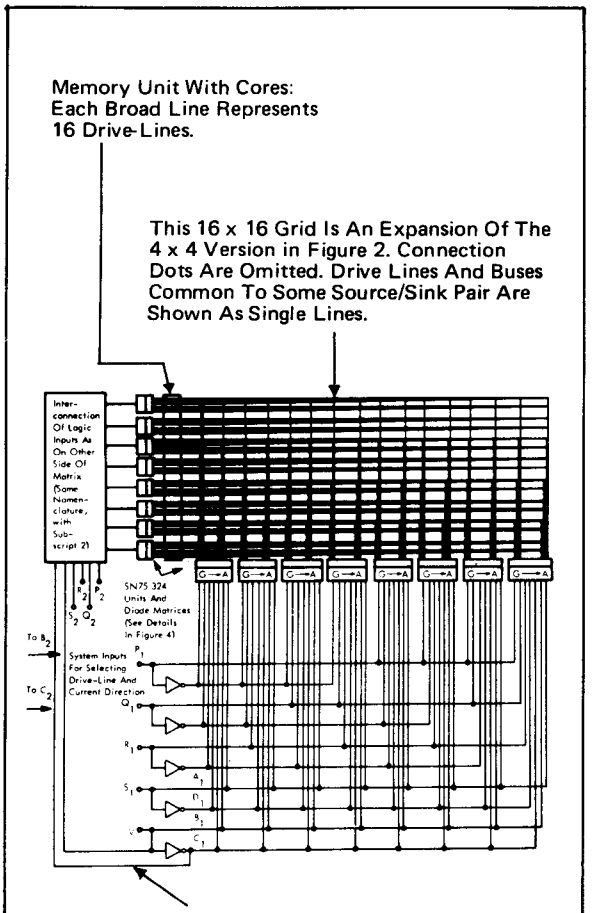


Figure 3. SN75324 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY, WITH HYPOTHETICAL LOGIC INTERCONNECTIONS TO SHOW INPUT FLEXIBILITY

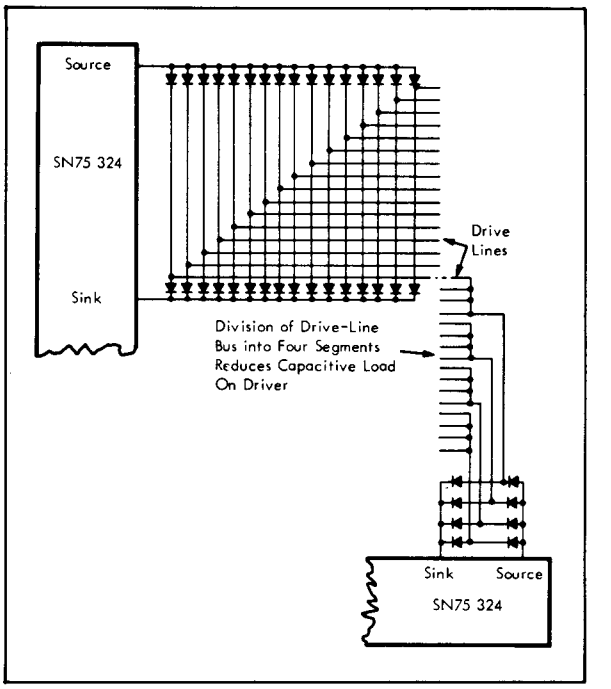


Figure 4. DETAILS OF CONNECTION OF DRIVE-LINES TO DRIVERS IN Figure 3.

A larger selection matrix is shown in Figures 3 and 4. The hypothetical interconnection of logic inputs demonstrates one way to take advantage of the multiple logic inputs of the SN75324.

Regardless of the particular line-selection and logic scheme, the SN75324 can be densely mounted on printed-wiring boards along with monolithic diode arrays and IC logic packages. The result normally is a system that is cheaper, faster, smaller, more reliable, and simpler to connect than a conventional discrete transistor-transformer version.

Logic Input from 74 TTL

Because of the high-noise environment in which the SN75324 is intended to operate, the input logic levels have been purposely designed to be somewhat higher than standard 74 TTL logic levels, as compared below:

	54/74 TTL	SN75 324
$V_{out(0)}$	0.4 V max.	— — —
$V_{out(1)}$	2.4 V min.	— — —
$V_{in(0)}$	0.8 V max.	1.0 V max.
$V_{in(1)}$	2.0 V min.	3.5 V min.
$V_{threshold}$	1.4 V typ.	2.3 V typ.

The higher logical 0 input level, $V_{in(0)}$ of the SN75324 guarantees a d-c noise margin of 600 mV when driven from 74 TTL. However, the higher $V_{in(1)}$ of the SN75324 (3.5 V) leads to some minor difficulties when using 54/74 TTL. The minimum guaranteed logical 1 level of 2.4 V at a 54/74 TTL output falls short of the 3.5-V minimum level required at the SN75324 input. However, this problem can be readily solved by the proper selection of a pull-up resistor at the gate output as shown in Figure 5.

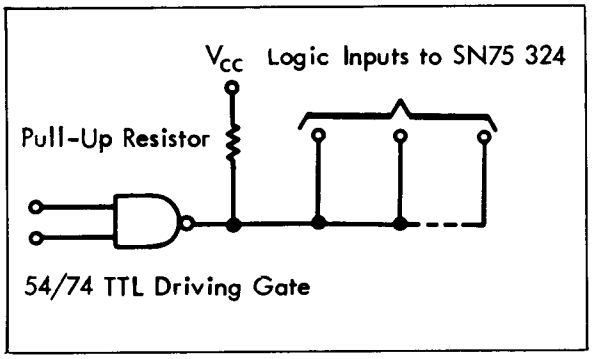


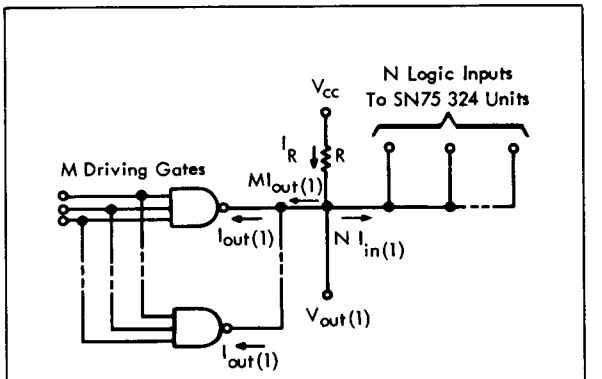
Figure 5. INPUT TO SN75324 FROM 74 TTL USING PULL-UP RESISTOR

Because of the high logical 0 input current of the SN75324 (12mA for the timing inputs, 6mA for the address inputs), it may be desirable to drive the inputs from 74 TTL buffer gates (SN7440 or SN74H40) to assure adequate sink current capability. Each SN7440 buffer gate output is specified at 0.4 V maximum $V_{out(0)}$ at a sink current of 48mA. The $V_{out(0)}$ for the SN74H40 buffer gate is 0.4 V at a sink current of 60mA. If additional sink current is required, the inputs and outputs of both gates in the SN7440 or SN74H40 package may be paralleled for 96 and 120mA capability, respectively. (This parallel connection requires no significant sacrifice, if any, in switching characteristics, but the outputs of these gates should not be paralleled without also paralleling inputs. Otherwise one or both of the gates can be damaged because of the active pull-up or "totem-pole" output configuration.)

A large number of SN75324 inputs may also be driven from the output of any of several 74 TTL decode/drivers. For example, the output of the SN7445 BCD-to-Decimal Decode/Driver can sink 80mA at $V_{out(0)}$ of 0.9 V or sink 20mA at $V_{out(0)}$ of 0.4 V. Since the maximum $V_{in(0)}$ of the SN75324 is 1.0 V, the SN7445 can drive the SN75324 with a pull-up resistor.

When a pull-up resistor is used at the driving gate output, its value must be determined to ensure proper logic levels. The worst-case resistor values may be readily calculated using available driving gate data sheet information, as exemplified below.

The maximum resistor value is calculated to ensure that sufficient current is available when the driving gate output is high (off). This current must supply the SN75324 input as well as the driving gate output. For a logical 1, it is necessary to maintain 3.5 V minimum at the SN75324 input. A suggested method of calculating the maximum resistor value is shown in Figure 6. The minimum value of the resistor is calculated to ensure that its current plus that from the SN75324 inputs will not cause the output voltage $V_{out(0)}$ of the driving gate to exceed the maximum of 1.0 V. (See Figure 7).



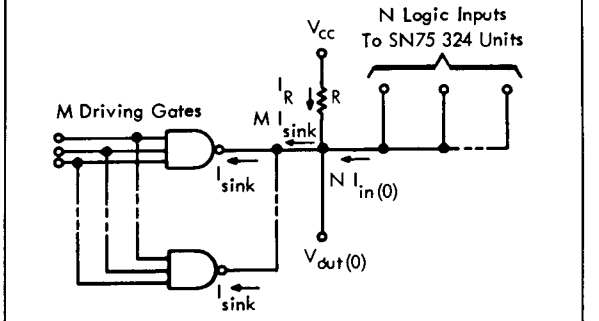
Voltage across R = $V_R = V_{CC}$ (min) − $V_{out(1)}$

Current through R = $I_R = M\ I_{out(1)} + N\ I_{in(1)}$

Therefore $R_{(max)} = \dfrac{V_{CC}\ (min) - V_{out(1)}}{M\ I_{out(1)} + N\ I_{in(1)}}$

where $V_{out(1)}$ = 3.5 V minimum to drive SN75 324 input
$I_{out(1)}$ = 250 µA maximum for 74 TTL gate output
$I_{in(1)}$ = 100 µA maximum for SN75 324 timing inputs
= 200 µA maximum for SN75 324 address inputs
M = number of parallel driving gates
N = number of parallel SN75 324 inputs

Figure 6. CALCULATION OF MAXIMUM VALUE OF PULL-UP RESISTOR IN Figure 5.



Current in resistor = $I_R = M\ I_{sink} - N\ I_{in(0)}$

Voltage across resistor = $V_R = V_{CC} - V_{out(0)}$

$$R_{(min)} = \frac{V_{CC} - V_{out(0)}}{M\ I_{sink} - N\ I_{in(0)}}$$

where $I_{in(0)}$ = 6 mA maximum for address inputs
$I_{in(0)}$ = 12 mA maximum for timing inputs
I_{sink} = maximum specified sink current of driving gate
$V_{out(0)}$ = maximum specified "0" level output voltage of the driving gate (≤1.0 V), which is 0.4 V for 74 TTL
M = number of parallel driving gates
N = number of parallel SN75 324 inputs

Figure 7. CALCULATION OF MINIMUM VALUE OF PULL-UP RESISTOR IN Figure 5.

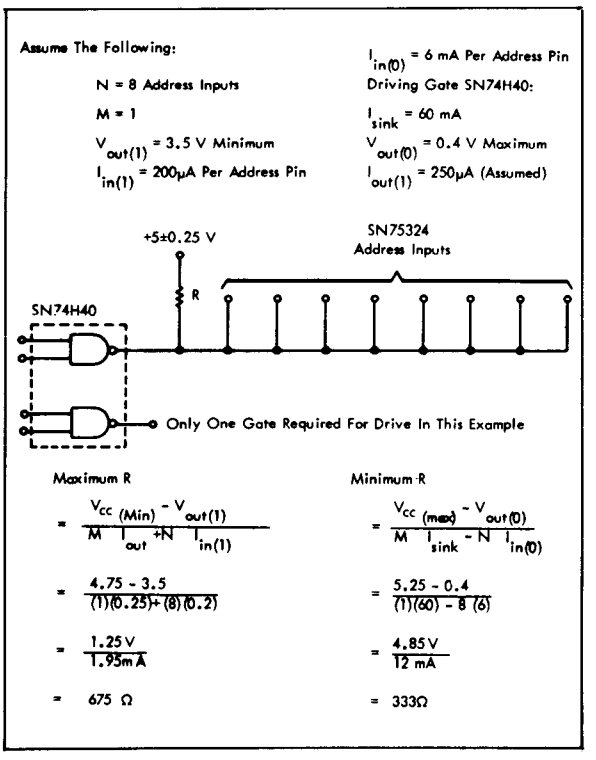


Figure 8. SAMPLE CALCULATION OF PULL-UP RESISTOR VALUE FOR SN74H40.

After determining the worst-case minimum and maximum pull-up resistor values, any value between the limits may be selected. (Obviously, the calculated minimum value must be below the calculated maximum value to be practical). Selecting a resistor value near the minimum limit will raise the logical 1 voltage and thereby improve the logical 1 noise margin.

An example of an SN74H40 buffer gate driving eight SN75324 address inputs is shown along with sample calculations in Figure 8. If, in this example, a value of 400 Ω is selected for the pull-up resistor, theguaranteed logic levels at the SN75324 inputs are 0.4 V maximum for $V_{in(0)}$ and 4.0 V minimum for $V_{in(1)}$. This resistor results in guaranteed d-c noise margins of 600mV at thelogical 0 level and 500mV at the logical 1 level at worst-case conditions.

Applications of the SN75325 Memory Driver

This device has the same use as the SN75324 but does not incorporate the decode facility, however, it is capable of sinking (sourcing more current, viz (600mA.) An SN74154 can be used to provide the required decode function. Apart from this, the applications of the SN75325 are similar to those of the SN75324.

Peripheral Drivers

TYPE	SN75450B	SN75451B	SN75452B	SN75453B	SN75454B
Features	Two TTL gates and two high current transistors on one chip. Each transitor sinks 300 mA of current and has a minimum collector-emitter breakdown voltage of 30 V.				
	* Two Uncommitted Transistors	* 8-pin Package	* AND Gates	* NOR Gates	* OR Gates
Applications	* Lamp Driver * Relay Driver * MOS Driver * Line Driver	* Lamp Driver * Relay Driver	* Lamp Driver * Relay Driver	* Lamp Driver * Relay Driver	* Lamp Driver * Relay Driver
No. of Pins	14	8	8	8	8

General Considerations

1. Figure 1 shows a typical load condition for a circuit using the 75450 range of integrated circuit peripheral drivers. Inductance will always be present in the load, since even a few inches of wire may have sufficient inductance to cause transistor breakdown under certain conditions. A low inductance decoupling capacitor will assist in reducing supply rail inductance in many applications. A fast catching diode with good overshoot characteristics such as the IS951 is essential for highly inductive loads, such as relays. This precaution should not be necessary for lamp driving, but may well assist operation with certain circuit layouts. A capacitance from the device output to ground will almost certainly be necessary for lamp driving from a supply greater than 20 volts. It is important that the natural resonant frequency of the load is such that the device output transistor is firmly off with a BV_{CES} breakdown characteristic before the output has risen above approximately 22 volts. Quite small values of total capacitance are normally needed to ensure this condition (where $dV/_{dt} <$ 1 V/ns); even PCB stray capacitance may be sufficient.
2. Figure 2 defines an unconditional maximum safe operating area for all devices in the range under any load conditions within data sheet specification, provided that a catch diode is present for highly inductive loads. Below 10 volts a catch diode is unnecessary. Dependent upon load characteristics, a catch diode may be unnecessary up to

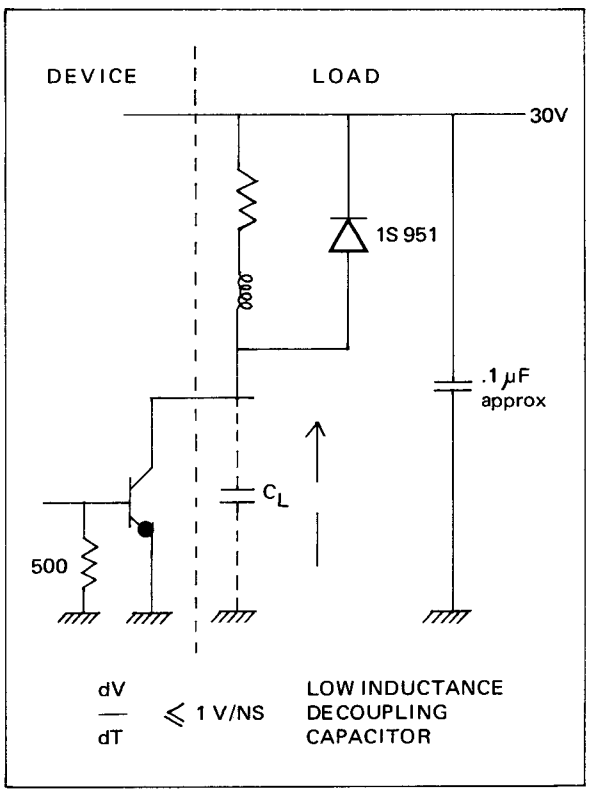


Figure 1.

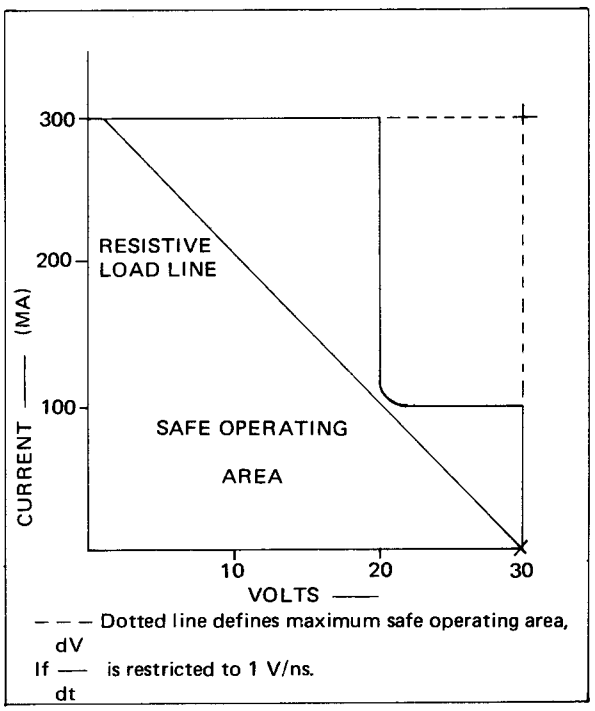


Figure 2. SAFE OPERATING AREA CONSIDERATIONS

about 17 or 18 volts. The dotted area of Figure 2 defines safe operating area conditional upon the rate of rise of output being less than 1 V/nS.

Safe operating area considerations must, of course, be consistent with the maximum power dissipation requirements of the package.

Applications of the SN75450B Series Peripheral Drivers SN75450B

A TTL output connected to a discrete power transistor provides a simple straightforward circuit for driving relays, small solenoids, incandescent lamps or low-impedance lines.

The TTL gate and the power transistor can be replaced with a System 74 integrated circuit driver, the SN75450B. The SN75450B circuit is shown in Figure 1. It contains two standard 74 TTL NAND gates and two 500mA NPN transistors. The NAND gates are conventional TTL gates operating from a supply voltage of +5 V and having a typical propagation delay of 10 ns with an average power dissipation of 10 mW per gate.

The SN75450B can be used to great advantage in many output interface situations. Although the SN75450B is primarily designed as a relay or lamp driver, it is extremely versatile and is useful in a wide variety of applications. Table 1 lists some of the possible uses of the SN75450B.

This versatility is possible because of the pin arrangement on the SN75450B package. Power supply and ground are the corner pins and allow for easy board layout. The NAND gate outputs and the transistor bases are adjacent since many applications require direct connection of these terminals. Also the emitters, ground and chip substrate are placed close to one another to permit easy interconnections. The chip substrate is not connected to ground, as is normal in TTL circuits, to permit the transistors to operate at a level more negative than system ground. The substrate pin is always connected by the board interconnection pattern to the most negative d-c voltage used in the application. This prevents interaction of components by reverse-biased isolation junctions.

The following typical circuits show various applications of the SN75450B series.

TABLE 1

SN75450B CIRCUIT APPLICATIONS

Dual Lamp Driver	SCR Gate Driver
Dual Relay Driver	Super TTL Gate With 250-mA Sinking Ability
Gated Comparator	Dual-Channel Single-Ended Line Driver
Floating Switch	Memory System Current Sink
Dual MOS-to-TTL Driver	Memory System Current Source
Dual TTL-to-MOS Driver	Film Memory Digit Driver
500-mA Sink-Driver	Core Memory Driver
Dual Linear Amplifier	Phase Detector
Dual Photo Switch (TTL Compatible Output)	DC-to-AC Converter
NAND Gate Schmitt (Timed Relay or Lamp Control)	Dwell Meter Driver
High Input-Impedance Low-Speed Schmitt with TTL Output	Tachometer
Dual High-Speed Gatel	MOS Memory Write Driver
Square Wave Generator	

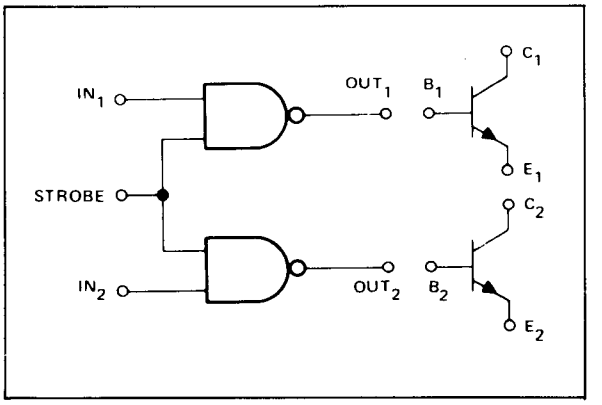


Figure 3.
FUNCTIONAL BLOCK DIAGRAM OF THE SN75450B

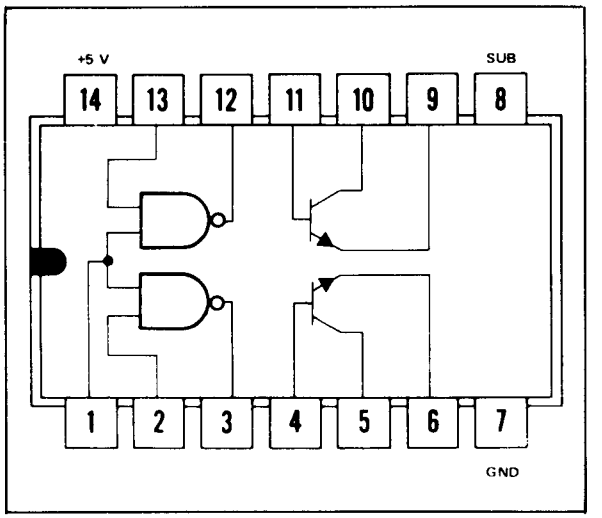


Figure 4. PACKAGE CONFIGURATION OF THE SN75450B

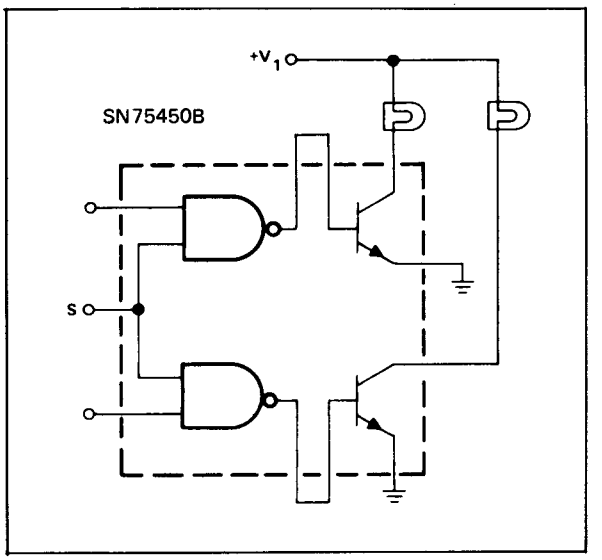


Figure 5. DUAL LAMP DRIVER USING SN75450B

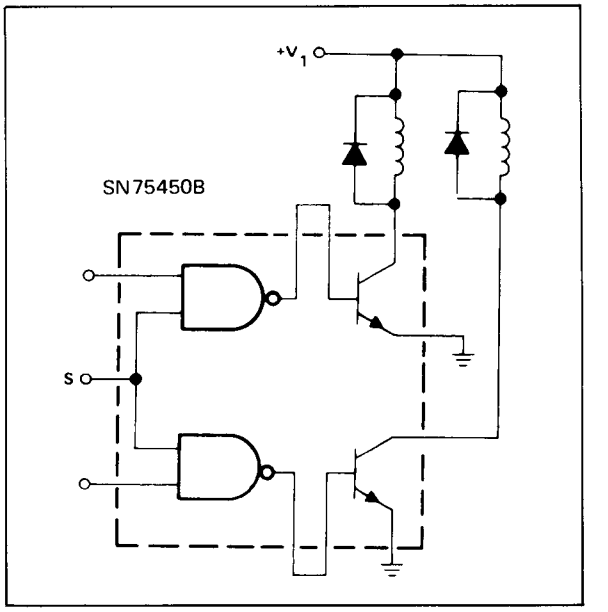


Figure 6. DUAL RELAY DRIVER USING SN75450B

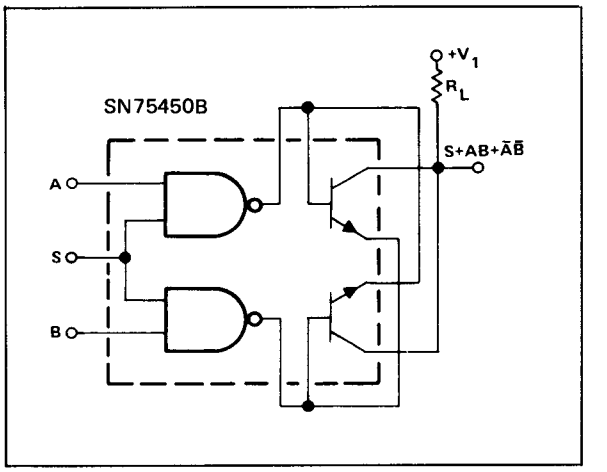


Figure 7. GATED COMPARATOR USING SN75450B

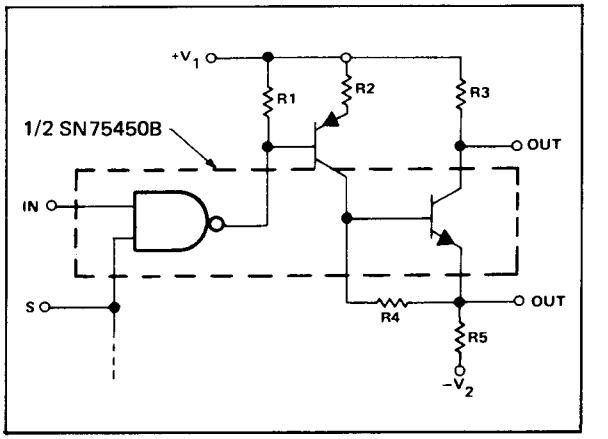


Figure 8. FLOATING SWITCH USING SN75450B

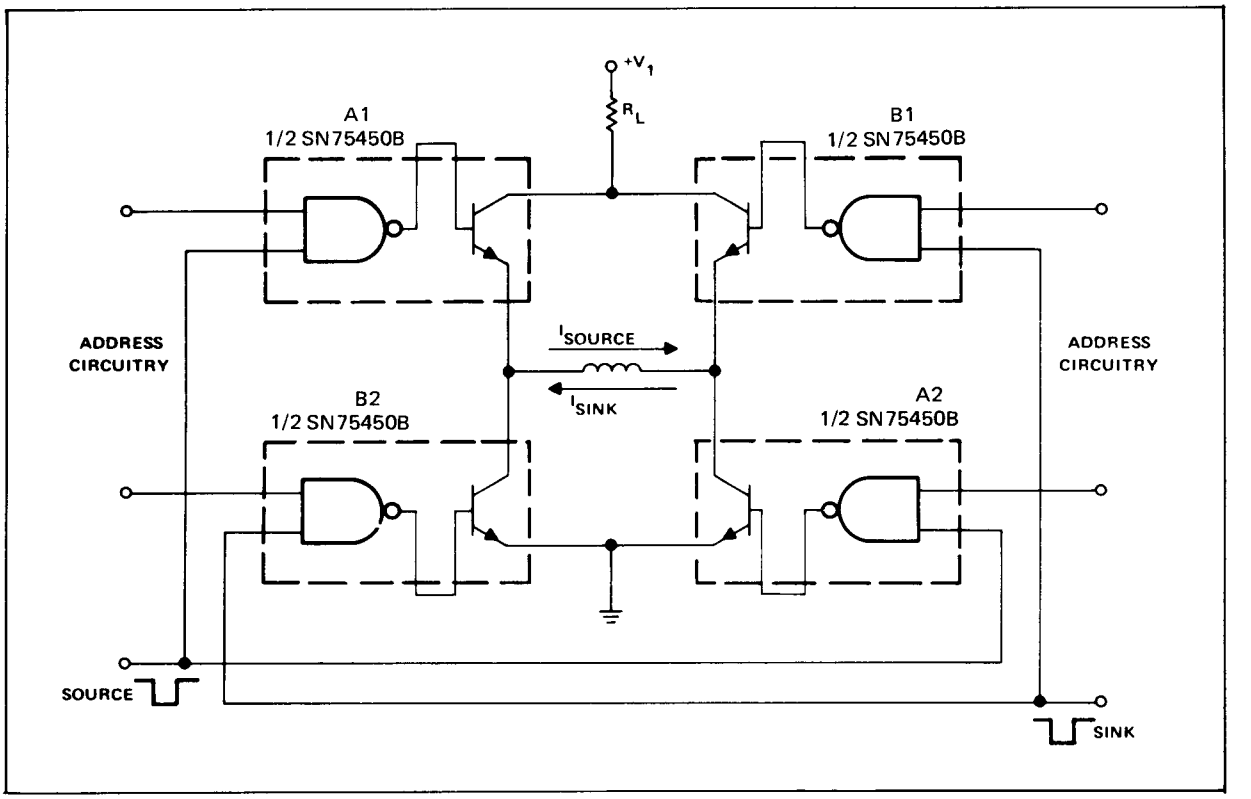


Figure 9. MEMORY DIGIT DRIVER USING SN75450B

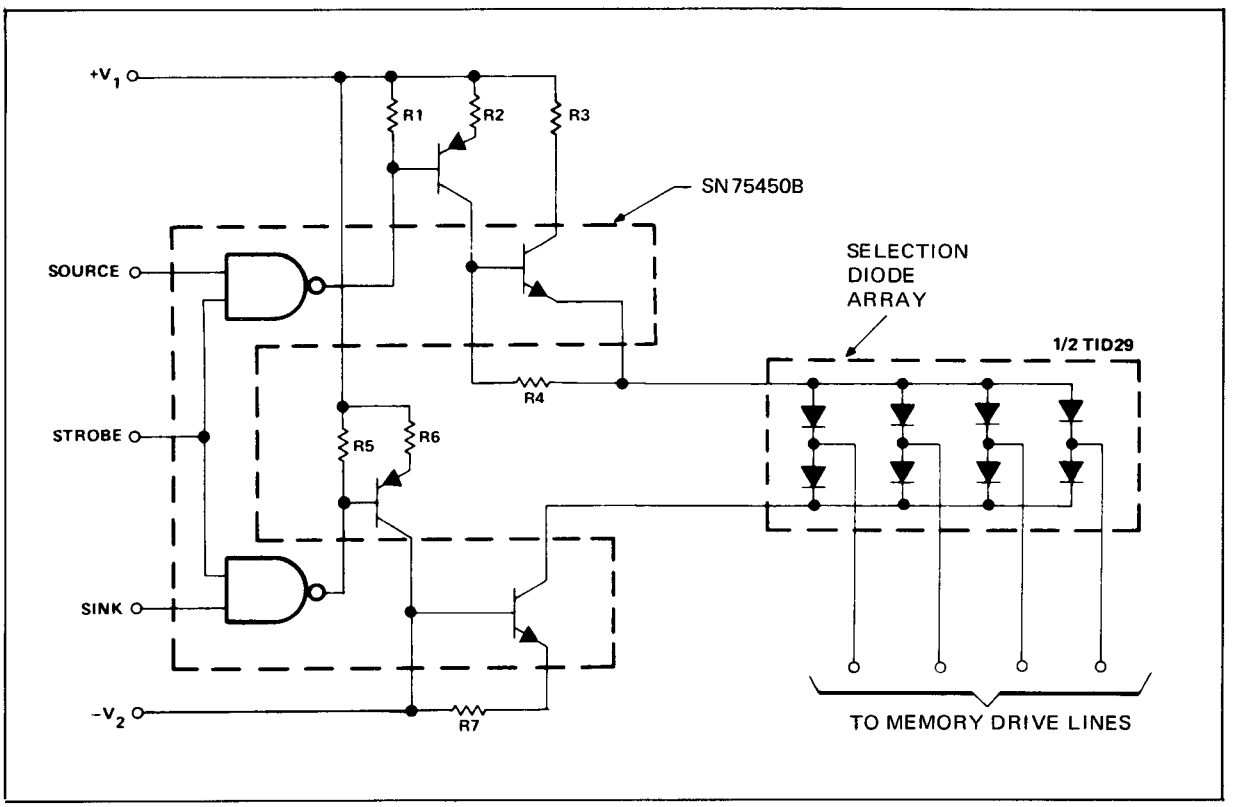


Figure 10. CORE MEMORY DRIVE USING SN75450B

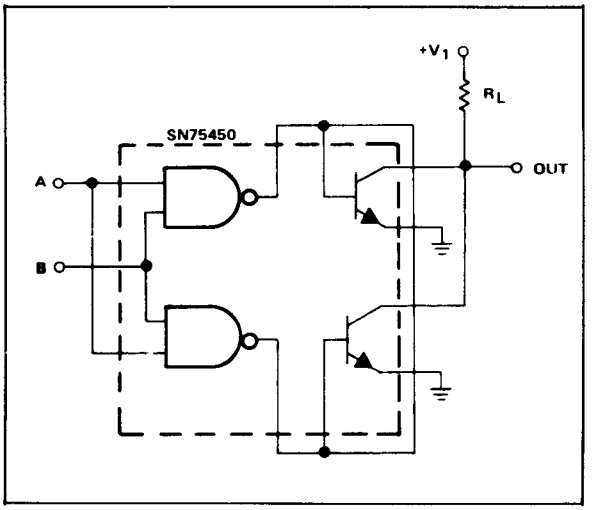


Figure 11. 500-mA SINK DRIVER USING SN75450B

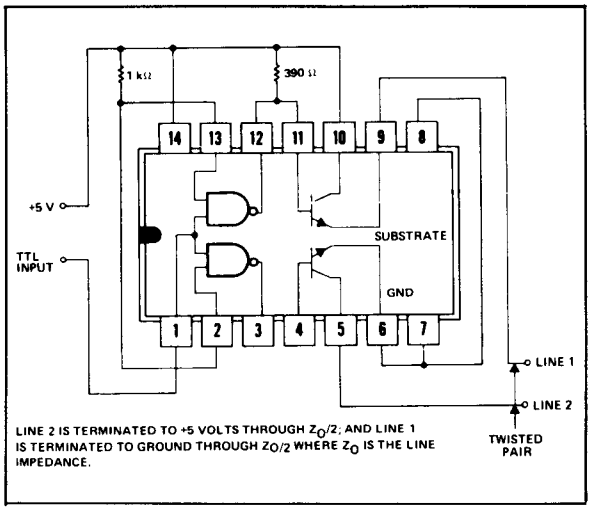


Figure 12. BALANCED LINE DRIVER USING SN75450B

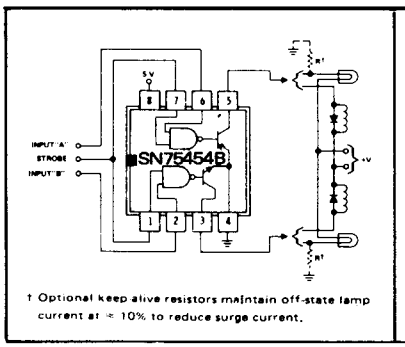


Figure 13. DUAL LAMP OR RELAY DRIVER

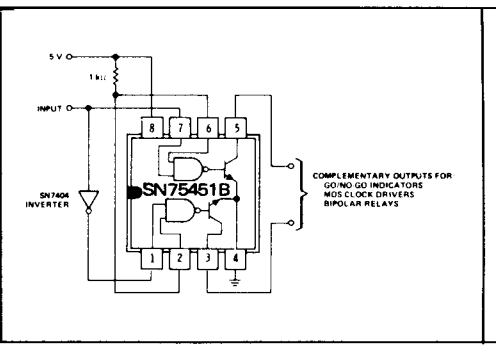


Figure 14. COMPLEMENTARY DRIVER

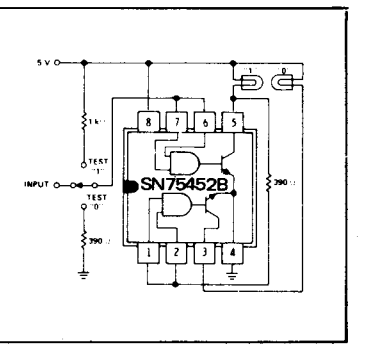


Figure 15. TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR

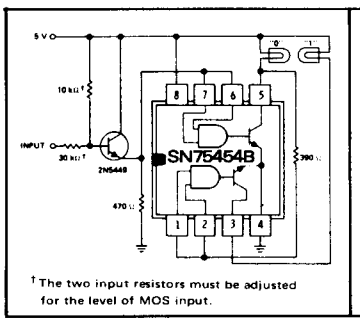


Figure 16. MOS NEGATIVE-LOGIC-LEVEL DETECTOR

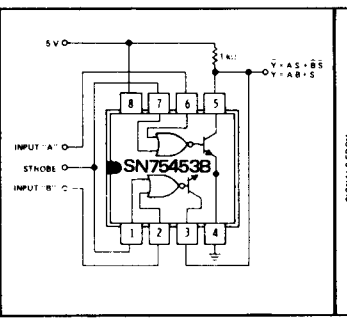


Figure 17. LOGIC SIGNAL COMPARATOR

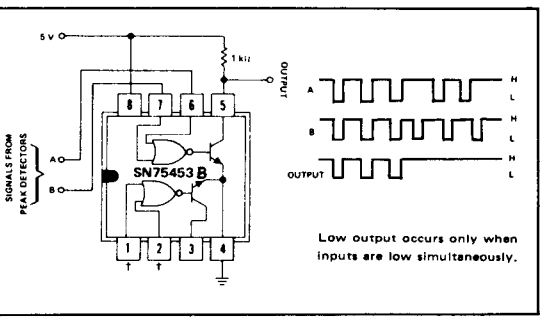


Figure 18. IN-PHASE DETECTOR

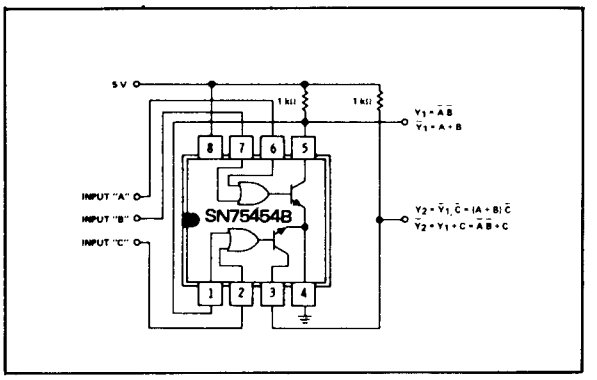


Figure 19. MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

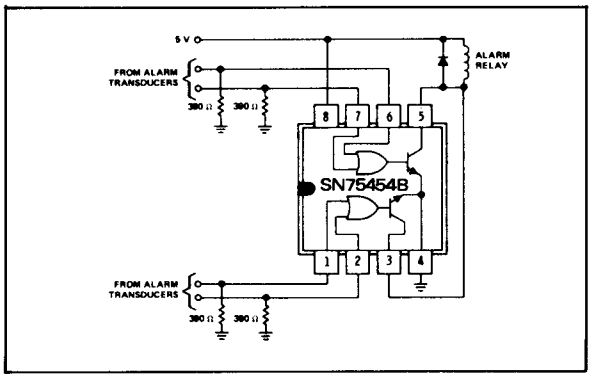


Figure 20. ALARM DETECTOR

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DESIGNERS' MANUAL

For further information on application of System 74 logic and interfacing devices the following Application Reports are recommended. They are individually priced as shown and are available from Data Sales MS21, Texas Instruments Ltd., Manton Lane, Bedford.

B10/12/14/16/19/21/25/26/30 Numerous TTL Applications

Various small reports covering: a Parallel Input Summing Counter, a Twenty-Four Hour Clock, A Ripple Counter Using TTL D-Type Flip-Flops, a 16-Bit Parallel Binary Comparator, a Serial Gray to Binary Converter, a Decade Counter with Unconditional Preset Facility, Dividing by Numbers Other than Ten with the SN7490N, Twenty-Four Hour Clock Using Only SN7490N Decade Counters and a Digital Phase Meter. PRICE 15p

B20/31 A to D and D to A Converters

The ADC converter described employs the 'Put and Take' method and is capable of converting a voltage lying between ±4V into an eight bit code in 10μs with an accuracy of ±15.6mV. The counter employs SN7474N D-type flip-flops, wideband differential amplifiers SN5510 and SN5511 are used in the comparator and complementary transistors are used to switch the ladder sections. An alternative FET switch circuit is given.

The DAC converter described was built to test analogue to digital converters. Correction procedure for errors arising from the ladder metal film resistor tolerances and device ON resistance is given. The 9 bit plus sign converter, using positive and negative references, could be set to give a maximum error of ± 200μV over the ±3.3V output range. The output was within 1mV of the required value within 6μs of clocking the input. Temperature effects are also considered. PRICE 10p

B50 Applications of the SN74121N TTL Integrated Circuit Monostable

Basic uses of the SN74121N high performance monostable circuit are given in this report, together with its application in a frequency to voltage converter system. FREE

B67 An I.C. Sequence Generator for Three Phase Stepping Motors

A circuit is described which produces a twelve state drive sequence for a stepping motor. Details of a discrete component 28V output stage and an auto stop facility are also included. PRICE 10p

B69 (or CA146) Applications of Line Drivers and Receivers

Two data transmission systems are described which make use of the SN55/75 109/10N line driver and the SN55/75 107/8N line receiver. One system is synchronous and the other non-synchronous. Some suggestions are made for the reduction of common-mode voltage spikes induced by the inhibit condition. PRICE 10p

B75 Solid State Switching Using Triacs and Thyristors

Although most of the solid state switching circuits in this report are single phase, some three phase and D.C. circuits are included. The actuation of solid state contactors by logic, a light beam and pilot switches are described. PRICE 10p

B78 A Programmable Synchronous Frequency Divider

This report describes an 8 bit shift register generator having a basic division ratio of 255. A means of modifying this basic count is described and a list of jump state addresses given, which allow all division ratios between 2 and 254 to be obtained. PRICE 5p

B82 (or CA 160) Binary Rate Multiplier

Device principles and internal operation of the Binary Rate Multiplier (BRM) are covered and it is shown how simple arithmetic operations can be performed with the minimum of control logic. Mathematical operations such as integration are covered. Examples are given where the BRM is used for solving differential equations and function generation with a minimum of control logic. PRICE 15p

B90 Use of TTL Integrated Circuits in Industrial Noise Environments

In certain environments, especially industrial ones, noise may be a serious problem. It can be caused by conditions internal or external to a TTL logic system. This report attempts to isolate the various possible sources of noise, show how, by careful design, problems can be avoided, and by systematic investigation how unwanted noise can be removed from pre-production equipment. PRICE 15p

B93 Schottky TTL

This report is intended to introduce someone who has some knowledge of TTL and emitter coupled logic to Schottky clamped TTL. It shows the increase in performance which can be obtained and the ease with which this is possible.

After a very brief explanation of the Schottky clamp action and the way speed is improved, the various performance parameters of the basic gate are examined. In the second half the manner in which these gate parameters affect system design is considered. PRICE 10p

B101 Binary to BCD and BCD to Binary Converters

Two converters based on the BIDEC system are described, one for converting pure Binary numbers to BCD and the other for BCD to Binary.

The converters have fast conversion speeds and both the circuit complexity and conversion time increase only in direct proportion to the number of bits converted. The shift/accumulate function is provided by an SN74199N universal 8 bit shift register and an SN74H52N gives fast look-ahead in the binary to BCD circuit. PRICE 5p

B102 TTL Counters and Registers

Descriptions of complex 74 Series TTL registers and counters are given followed by numerous practical circuits using them. To help the designer use the series further the functional analysis required to construct the circuits is provided where needed. This report was originally CA102 'TTL Integrated Circuits: Counters and Shift Registers', but has been completely revised and edited and a reference system gives new approaches and devices now available. PRICE 10p

B115 SN54/74184 BCD to Binary SN54/74185A Binary to BCD Code Converters

The SN54/74184 and SN54/74185A are BCD to binary and binary BCD converters which are derived from the SN54/7488 custom MSI 256 bit Read Only Memory. Both devices may be cascaded to perform conversion of any number of decades or any number of bits. This report contains a description of the SN54/74184 and SN54/74185A device characteristics and explains how the devices are cascaded. Circuit diagrams for up to six decade BCD to binary and up to 20 bit binary to BCD converters are included. PRICE 15p

B121 Using Optoelectronics

Many simple applications are given showing how to best use optoelectronic devices. These include visible and infra-red sensors and emitters, optically coupled isolators, modules, and visible displays. Although the examples are specifically written about low-cost high volume devices which are most readily available, the techniques can be applied to all types. FREE

B124 TTL – From the Beginning

Previous TTL applications reports have assumed that the reader is familiar with TTL and only needs an explanation of a new technique or circuit function. The newcomer to the subject has always been thrown in at the deep end. What they have cried for, those that have not sunk, is something more basic. This report is designed to assist the non-swimmer and give him an explanation of TTL from the beginning. PRICE 20p

CA101 Operation and Use of Series 7520N Sense Amplifiers

Series 7520 integrated circuit sense amplifiers are designed for use in coincident memory applications where discrimination input information is based on input signal amplitude and position in time, regardless of signal polarity. The characteristics of these sense amplifiers are described and a variety of applications are presented. FREE

CA129 TTL Design Cases and Guidelines

Seven standard 54/74 TTL "design cases" are presented here, each consisting of a problem frequency encountered and its solution (reprinted from EDN magazine's "Customer Engineering Clinic" of January through April, 1969). Also included are rule-of-thumb answers to 21 frequently asked questions regarding practical use of standard 54/74 TTL. PRICE 15p

CA130 Line Drivers and Receivers SN55107 Series

This series of monolithic integrated circuits are designed to transmit data in 54/74 TTL systems rapidly over long lines subject to noise. Here, the operation and use of the circuits are described and many applications are outlined. PRICE 20p

CA132 TTL Data Selectors

Illustrations of the wide variety of functions which the SN54/74 150/1/2 range of data selectors can perform are given, e.g. random and sequential data selection, parallel to serial conversion, multiplexing to one and multiple lines as character generators, and implementing logic functions.

one and multiple lines as character generators, and implementing logic functions. PRICE 15p

CA143 SN54/74154 Decoder/Demultiplexer

This integrated circuit is a 4-line-to-16 line decoder or 1-line to-16-line demultiplexer. Its characteristics and several applications are discussed in this report. PRICE 5p

CA148 TTL 50MHz Flip Flops SN74H 100 Series

A general description of the series is followed by sections on Synchronous Operation and Switching Speed, Operating Frequency, Clock Skew Protection, Asynchronous Operation and Switching Speed, D-C Characteristics and Practical Operating Conditions. Applications discussed are their use as Counters and Shift Registers, Synchronising an Asynchronous Input and a Frequency and/or Phase Comparator. PRICE 15p

CA153 – 7 Selected Optoelectronic Application Reports

Reports Included are:-

CA153 Optoelectronic fault indicator for logic circuits.
CA154 Optoelectronic Read Head for Punched cards and tape.
CA155 Injection laser diode fundamentals.
CA156 Optically coupled isolators in circuits
CA157 Measuring light emitting diode output.
PRICE 25p

NA46 Bipolar Read Only Memories

Device description and characteristics are followed by application details where various possible organisations of the ROM are explained, e.g. increasing length of words, memory capacity, etc. The use of the SN7488 as a Boolean Function Generator, Code Converter, Sequential Function Generator and Function Table are then described in some detail using truth tables and a flow diagram where necessary. PRICE 15p

A Summary of all Application Reports is also published by Texas Instruments and is available free of charge on request.

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Most of the material used in the books has been written by engineers in the Texas Applications Laboratory at Bedford. Other material has been drawn from T.I. Laboratories throughout Europe and the U.S.A. Together they present a series of integrated papers which give a comprehensive treatment to both the theory *and practical* details of the *subjects* covered.

VOLUME 1 (first published in 1972) is written with a broad industrial bias and is divided into four sections which cover applications for TTL Integrated Circuits, Power Transistors,, Audio Circuits and

Circuits and Power Control using Triacs, Thyristors and unijunction transistors.

VOLUME 2 (published June 1973) has been compiled from the most up-to-date material available and is divided into three sections dealing with Digital I.C.'s., operational amplifiers and Optoelectronics. Each section is preceded by an introductory chapter explaining the techniques of using these devices.

Complete the order form at the back of this manual.

These books are therefore of use both to the moderately advanced student and the designer in industry who can apply the circuits as they stand or adapt them as required.

Both volumes are massively illustrated with circuit diagrams, graphs, oscilloscope test traces, circuit board layout and data tables. The text matter in both books runs to over 200 pages and they are both bound with hardback covers.

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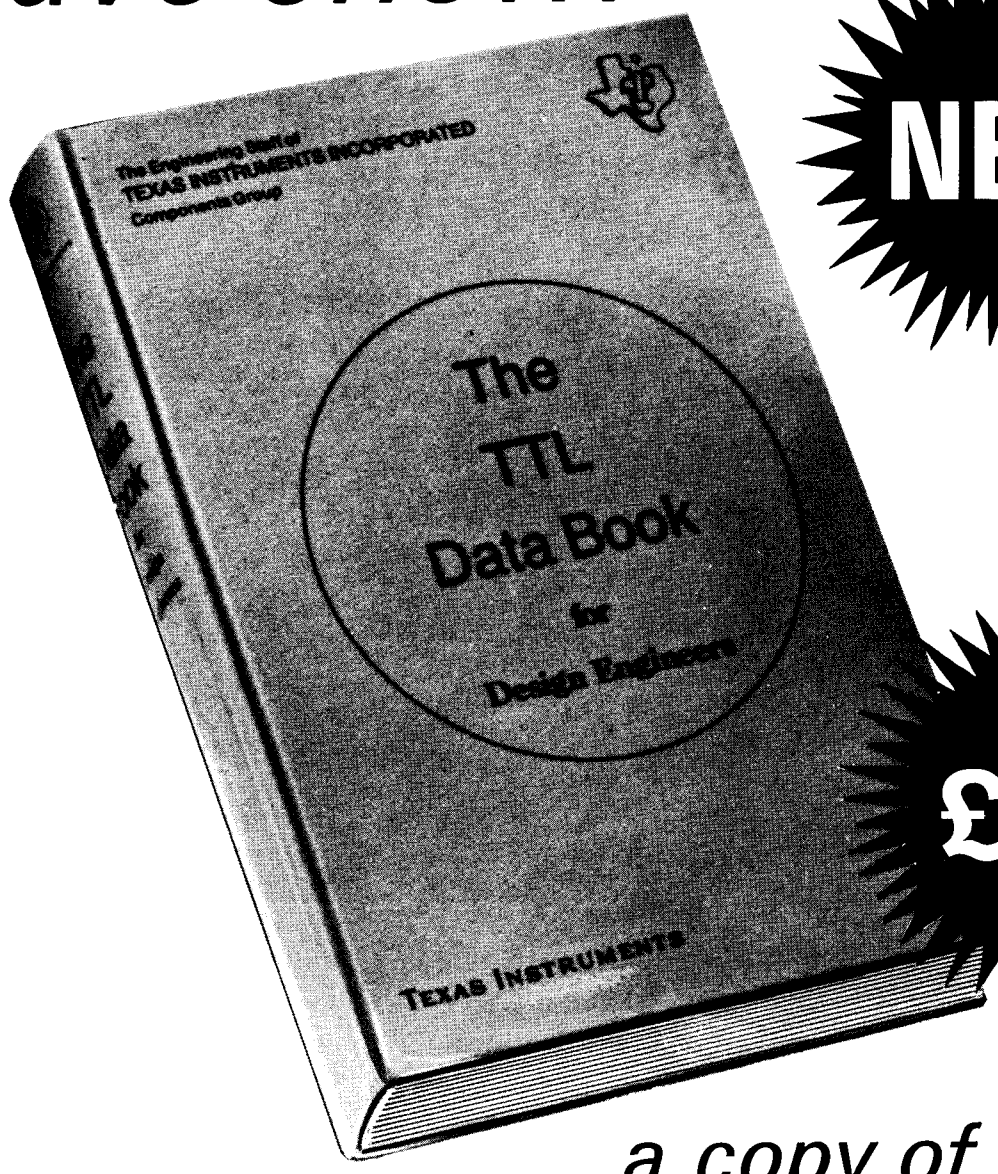

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A vital part of the System 74 concept, the new TTL Data Book from Texas Instruments provides comprehensive specifications on T.I.'s five families of 54/74 TTL I.C.'s. This 640-page hard-bound book includes parametrical data on standard Series 54/74, the high-speed Series 54H/74H, the low power Series 54L/74L, the Schottky-clamped Series 54S/74S and low power Schottky Series 54LS/74LS. Also included are radiation-hardened and beam lead circuits and TTL high performance random access memories, as well as Series 29000 and Series 29 300/39 300.

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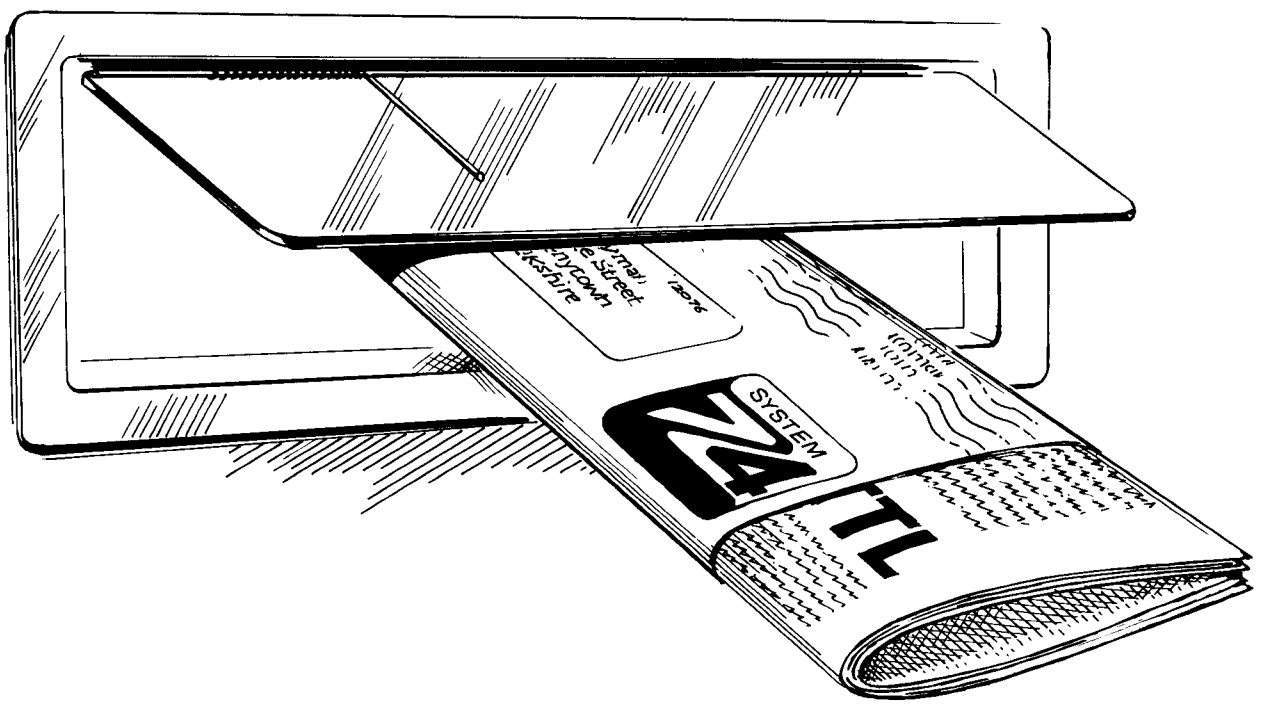

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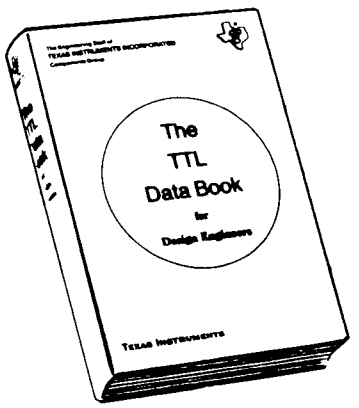

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