MSM38128ARS

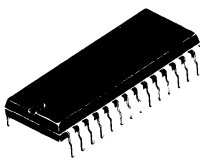
16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

GENERAL DESCRIPTION

The MSM38128ARS is an N-channel silicon gate MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

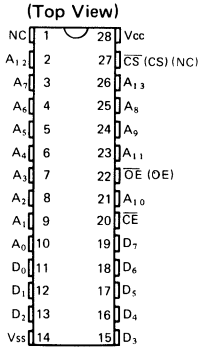
FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

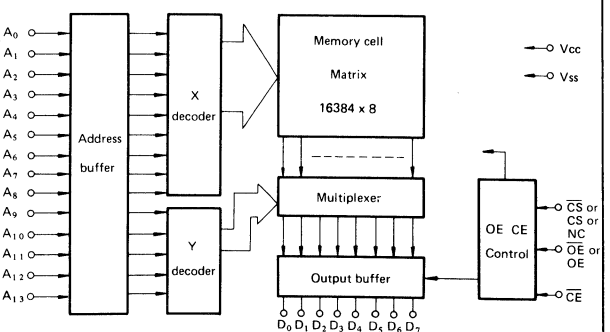
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the $\overline{OE}$ active level and $\overline{CS}$ active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc = Max.	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

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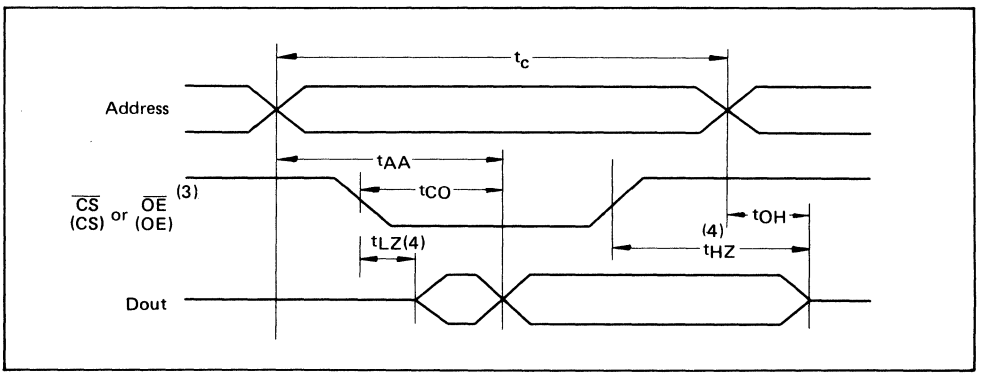
READ CYCLE

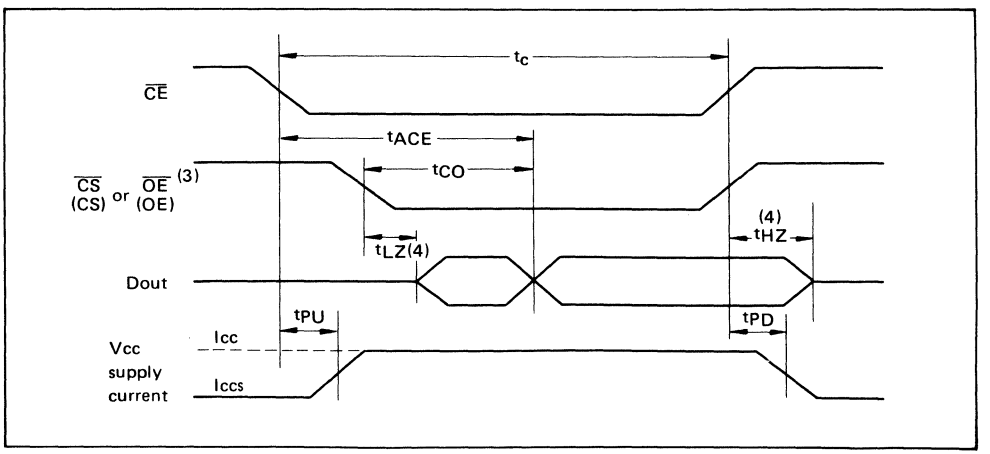
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	–		ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–		ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{Lz} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{Hz} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{Hz} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V