# HM51256P Series
# HM51256CP Series

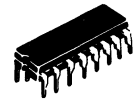
Preliminary

**262144-word × 1-bit CMOS Dynamic Random Access Memory**

## ■FEATURE

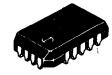
- 262, 144 word x 1 bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 100/120/150ns
  - Address access time: 45/55/70ns
- Cycle time
  - Random read/write cycle time: 180/210/250ns
  - High speed page mode cycle time: 55/65/80ns
- Lower power
  - Standby: 11mW
  - Active: 330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control

HM51256P Series



(DP-16B)

HM51256CP Series



(CP-18)

## ■ABSOLUTE MAXIMUM RATINGS

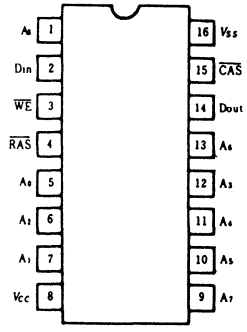
| | |
|---|---|
| Voltage on any pin relative to $V_{SS}$ | -1V to +7V |
| Operating temperature, Ta (Ambient) | 0°C to +70°C |
| Storage temperature | -55°C to +125°C |
| Short circuit output current | 50mA |
| Power dissipation | 1W |

| | |
|---|---|
| $A_0$~$A_8$ | Address Inputs |
| $\overline{CAS}$ | Column Address Strobe |
| Din | Data In |
| Dout | Data Out |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{WE}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| $A_0$~$A_7$ | Refresh Address Inputs |

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

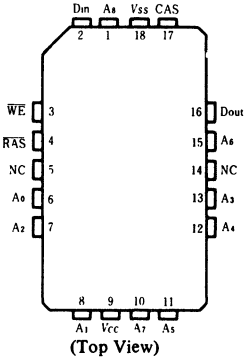
## ■PIN ARRANGEMENT

- HM51256P Series




(Top View)

- HM51256CP Series




(Top View)

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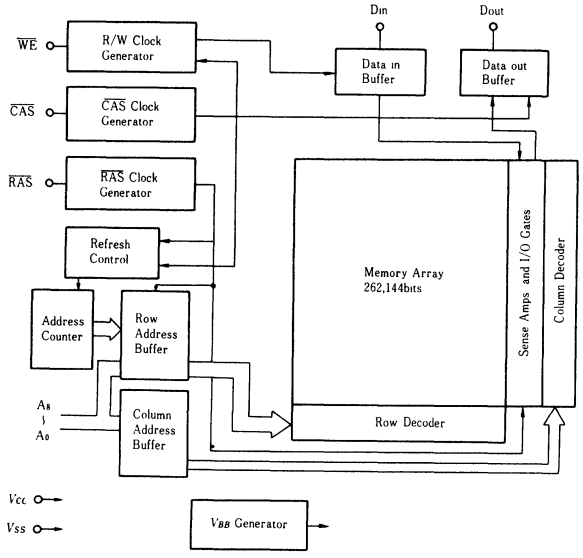
## ■ BLOCK DIAGRAM




## ■ RECOMMENDED DC OPERATING CONDITIONS ($Ta$=0 to +70°C)

| Parameter | Symbol | min | typ | max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input Low Voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note) 1. All voltages referenced to $V_{SS}$

## ■ DC ELECTRICAL CHARACTERISTICS ($Ta$=0 to +70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V)

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}$=min) | $I_{CC1}$ | — | 60 | — | 50 | — | 40 | mA | 1 |
| Standby Current ($\overline{RAS}$=$V_{IH}$, Dout=High Impedance) | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | |
| Refresh Current ($\overline{RAS}$ only Refresh, $t_{RC}$=min) | $I_{CC3}$ | — | 60 | — | 50 | — | 40 | mA | |
| Standby Current ($\overline{RAS}$=$V_{IH}$, Dout Enable) | $I_{CC4}$ | — | 6 | — | 6 | — | 6 | mA | 1 |
| Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, $t_{RC}$=min) | $I_{CC5}$ | — | 55 | — | 45 | — | 35 | mA | |
| Page Mode Supply Current ($\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ Cycling, $t_{PC}$=min.) | $I_{CC6}$ | — | 60 | — | 50 | — | 40 | mA | |
| Input leakage (0<$V_{in}$<7V) | $I_{LI}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output leakage (0<$V_{out}$<7V, Dout=Disable) | $I_{LO}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output levels High ($I_{out}$=−5mA) | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output levels Low ($I_{out}$=4.2mA) | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |

Notes) 1 $I_{CC}$ depends on output loading condition when the device is selected $I_{CC}$ max. is specified at the output open condition

## ■ CAPACITANCE ($V_{CC}$=5V±10%, $Ta$=25°C)

| Parameter | | Symbol | typ | max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input Capacitance | Address, Data-in | $C_{I1}$ | — | 5 | pF | 1 |
| | Clocks | $C_{I2}$ | — | 7 | | 1 |
| Output Capacitance | Data-out | $C_O$ | — | 7 | | 1, 2 |

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=$V_{IH}$ to disable Dout.

## ■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($Ta$=0 to +70°C, $Vcc$=5V±10%, $Vss$=0V)

### ● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 180 | – | 210 | – | 250 | – | ns | |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 70 | – | 80 | – | 90 | – | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 65 | 10000 | 75 | 10000 | 95 | 10000 | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 25 | – | 30 | – | 35 | – | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | – | 0 | – | 0 | – | ns | |
| Column Address Hold Time | $t_{CAH}$ | 20 | – | 25 | – | 30 | – | ns | |
| Column Address Hold Time to $\overline{RAS}$ | $t_{AR}$ | 75 | – | 90 | – | 110 | – | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 25 | 75 | 25 | 90 | 30 | 115 | ns | 8 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 20 | 55 | 20 | 65 | 25 | 80 | ns | 9 |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 25 | – | 30 | – | 35 | – | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 100 | – | 120 | – | 150 | – | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | – | 10 | – | 10 | – | ns | |
| Row Address Set-up Time | $t_{ASR}$ | 0 | – | 0 | – | 0 | – | ns | |
| Row Address Hold Time | $t_{RAH}$ | 15 | – | 15 | – | 20 | – | ns | |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 7 |
| Refresh Period | $t_{REF}$ | – | 4 | – | 4 | – | 4 | ms | |

### ● Read Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | – | 100 | – | 120 | – | 150 | ns | 2, 3 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | – | 25 | – | 30 | – | 35 | ns | 3, 4 |
| Access Time from Address | $t_{AA}$ | – | 45 | – | 55 | – | 70 | ns | 3, 5, 14 |
| Read Command Set-up Time | $t_{RCS}$ | 0 | – | 0 | – | 0 | – | ns | |
| Read Command Hold Time to $\overline{CAS}$ | $t_{RCH}$ | 0 | – | 0 | – | 0 | – | ns | |
| Read Command Hold Time to $\overline{RAS}$ | $t_{RRH}$ | 10 | – | 10 | – | 10 | – | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 45 | – | 55 | – | 70 | – | ns | |
| Output Buffer Turn-off Time | $t_{OFF}$ | 0 | 25 | 0 | 30 | 0 | 35 | ns | 6 |

### ● Write Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | – | 0 | – | 0 | – | ns | 10 |
| Write Command Hold Time | $t_{WCH}$ | 25 | – | 30 | – | 35 | – | ns | |
| Write Command Hold Time to $\overline{RAS}$ | $t_{WCR}$ | 80 | – | 95 | – | 115 | – | ns | |
| Write Command Pulse Width | $t_{WP}$ | 20 | – | 25 | – | 30 | – | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 25 | – | 30 | – | 35 | – | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 25 | – | 30 | – | 35 | – | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | – | 0 | – | 0 | – | ns | 11 |
| Data-in Hold Time | $t_{DH}$ | 20 | – | 25 | – | 30 | – | ns | 10, 11 |
| Data-in Hold Time to $\overline{RAS}$ | $t_{DHR}$ | 75 | – | 90 | – | 110 | – | ns | |

### ● Read-Modify-Write Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Read-Write Cycle Time | $t_{RWC}$ | 210 | – | 245 | – | 290 | – | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 100 | – | 120 | – | 150 | – | ns | 10 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 25 | – | 30 | – | 35 | – | ns | 10 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 45 | – | 55 | – | 70 | – | ns | 10 |

## ● Refresh Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP 12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CSR}$ | 10 | - | 10 | -- | 10 | - | ns | |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CHR}$ | 10 | | 10 | - | 10 | - | ns | |
| $\overline{RAS}$ Prechange to $\overline{CAS}$ Hold Time | $t_{RPC}$ | 15 | | 15 | -- | 15 | - | ns | |

## ● High Speed Page Mode Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| High Speed Page Mode Cycle Time | $t_{PC}$ | 55 | - | 65 | -- | 80 | - | ns | 18, 20 |
| High Speed Page Mode $\overline{RAS}$ Pulse Width | $t_{RAPC}$ | 65 | 75000 | 75 | 75000 | 95 | 75000 | ns | 19 |
| $\overline{RAS}$ to Second $\overline{WE}$ Delay Time | $t_{RSW}$ | 105 | | 125 | - | 155 | - | ns | |
| $\overline{CAS}$ Precharge Time | $t_{CP}$ | 15 | -- | 20 | - | 20 | - | ns | |
| Write Invalid Time | $t_{WI}$ | 10 | - | 15 | -- | 15 | - | ns | |
| Access Time from Column Precharge Time | $t_{CAP}$ | | 50 | - | 60 | - | 75 | ns | 20 |

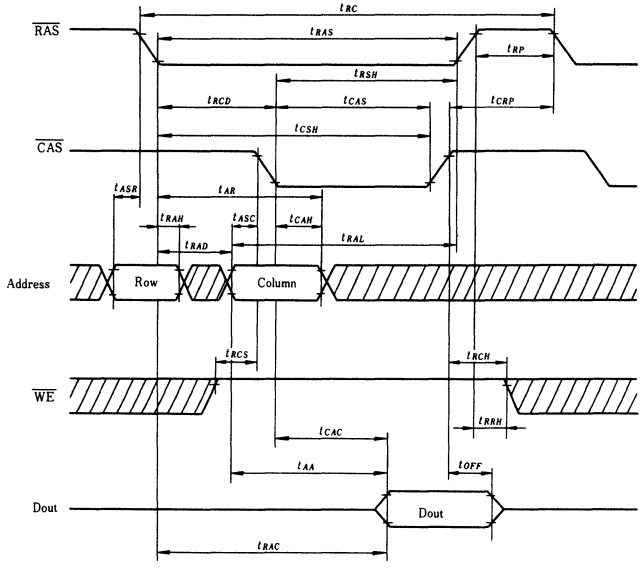
## ● High Speed Page Mode Read-Modify-Write Cycle

| Parameter | Symbol | HM51256P/CP-10 | | HM51256P/CP-12 | | HM51256P/CP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| High Speed Page Mode Cycle Time on Read-Write | $t_{RWPC}$ | 95 | - | 115 | - | 145 | - | ns | 12 |
| Access Time from Previous $\overline{WE}$ | $t_{PWA}$ | - | 90 | - | 110 | - | 140 | ns | 3, 13 |
| Previous $\overline{WE}$ to Column Address Delay Time | $t_{WAD}$ | 25 | 45 | 30 | 55 | 35 | 70 | ns | 15 |

Notes:
1. AC measurements assume $t_T$ = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value show in this table, $t_{RAC}$ exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
8. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only, if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
9. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a Reference point only, if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
10. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle, if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. $t_{RWPC}$ (min) = $t_{AWD}$ (min) + $t_{WAD}$ (max) + $t_T$.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If $t_{WAD}$ is greater than the maximum recomended value shown in this table, $t_{PWA}$ exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the $t_{WAD}$ (max) limit insures that $t_{PWA}$ (max) can be met, $t_{WAD}$ (max) is specified as a reference point only, if $t_{WAD}$ is greater than the specified $t_{WAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
16. An intial pause of 100$\mu$s is required after power-up then execute at least 8 initialization cycles.
17. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. Assumes that $t_{ASC} = tCP - 5$ ns.
19. $t_{RAPC}$ defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
20. Access time is determined by the longer of $t_{AA}$ or $t_{CAC}$ or $t_{CAP}$.

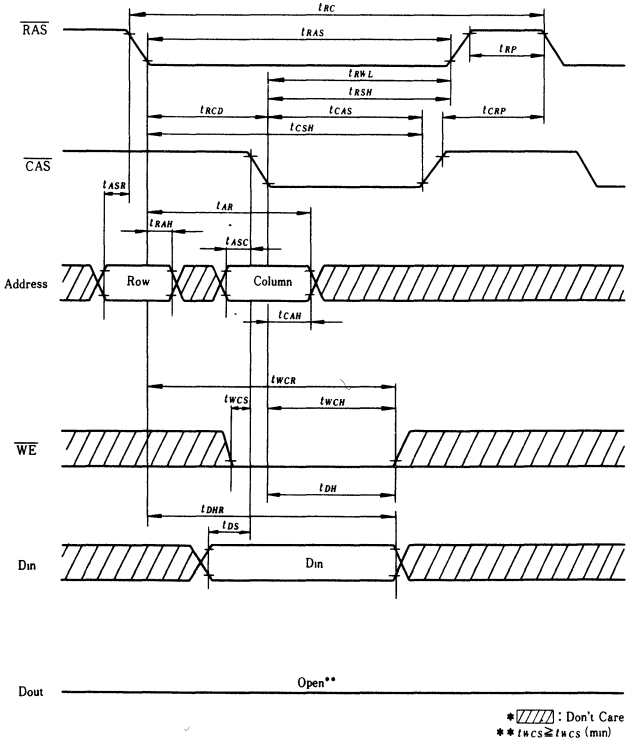
## ■TIMING WAVEFORMS

### ● Read Cycle



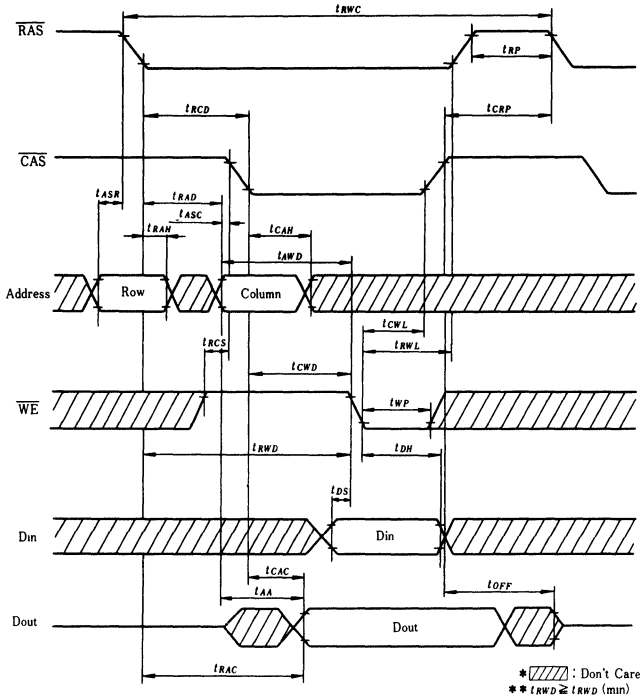

### ● Write Cycle

*▨ : Don't Care

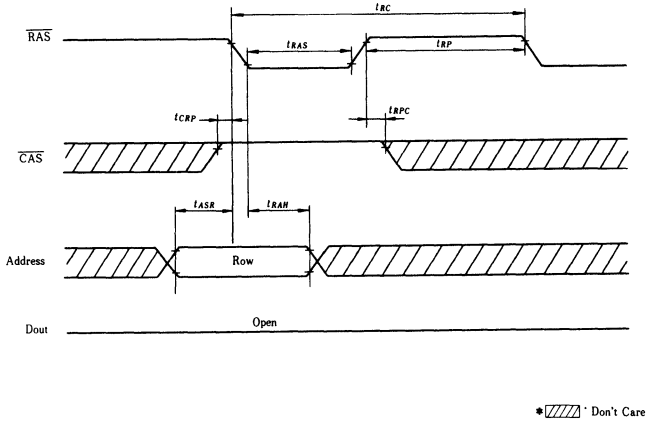



*▨ : Don't Care
** $t_{WCS} \geq t_{WCS}$ (min)

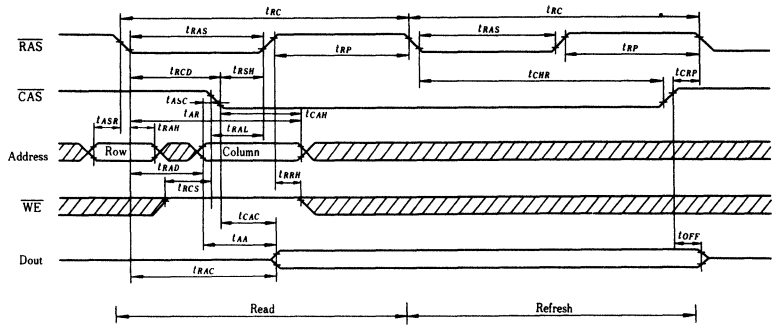
## ● Read Modify Write Cycle




## ● $\overline{\text{RAS}}$ Only Refresh Cycle

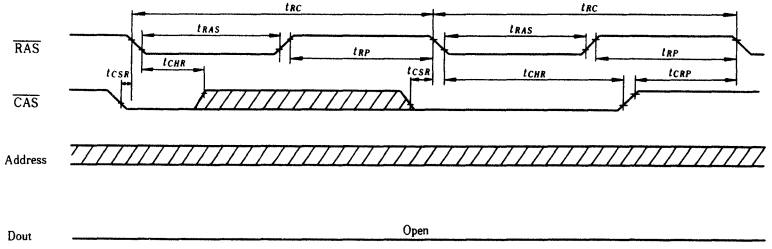


## ● Hidden Refresh Cycle



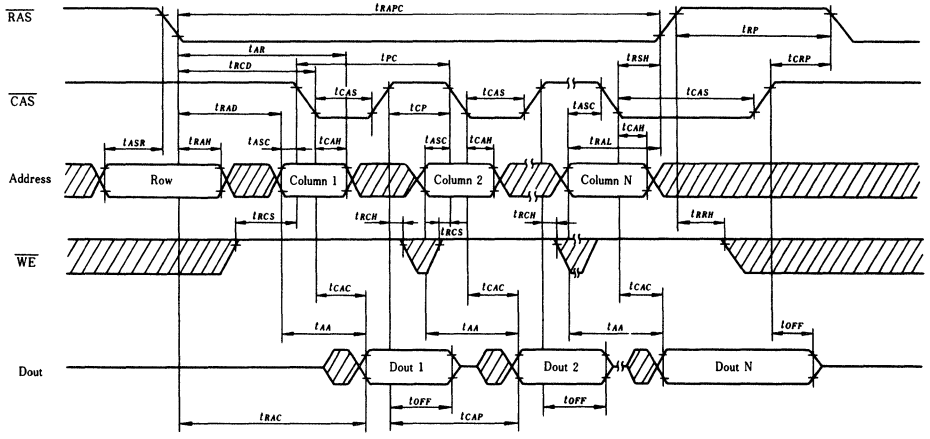

*▨: Don't Care

## ● CAS Before RAS Refresh Cycle



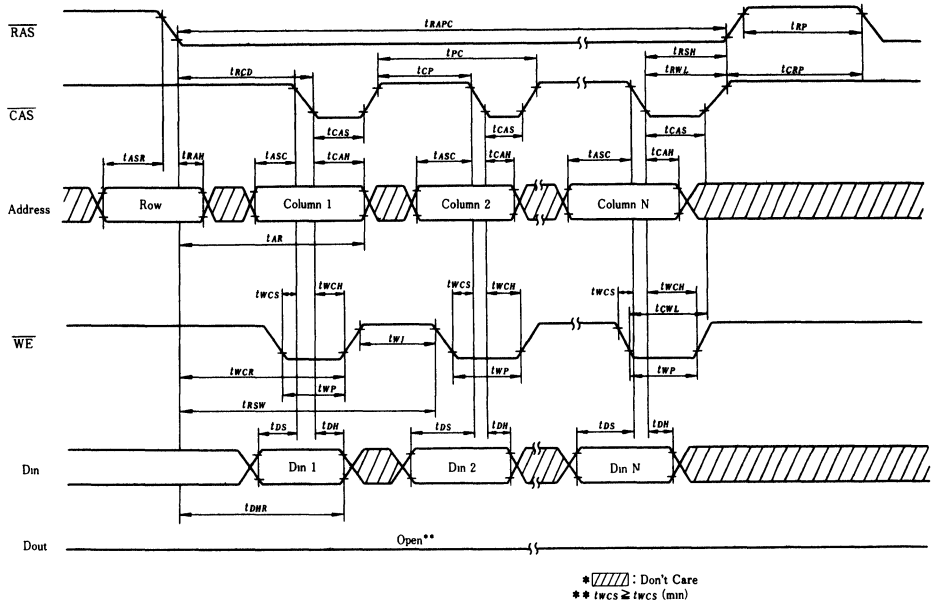

*▨: Don't Care

## ● High Speed Page Mode Read Cycle

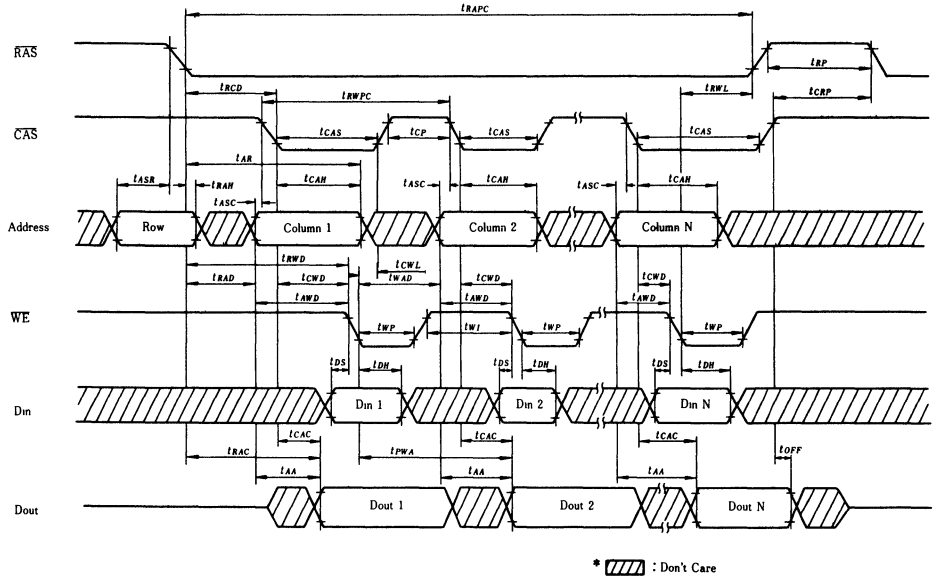



*▨: Don't Care

## ● High Speed Page Mode Write Cycle




## ● High Speed Page Mode Read Modify Write Cycle

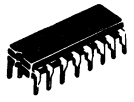


# HM51256LP Series
# HM51256LCP Series

Preliminary

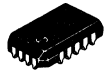
**262144-word x 1-bit CMOS Dynamic Random Access Memory**

HM51256LP Series



(DP-16B)

HM51256LCP Series



(CP-18)

## ■FEATURE

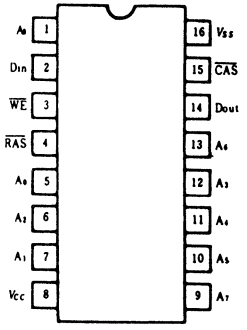
- 262, 144 word x 1-bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Policide process high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 100/120/150ns
  - Address access time: 45/55/70ns
- Cycle time
  - Random read/write cycle time: 180/210/250ns
  - High speed page mode cycle time: 55/65/80ns
- Lower power
  - Standby: 11mW (TTL level), 1.1 mW (CMOS level)
  - Active: 330/275/220mW
  - Data Retention Current: 300μA/$t_{REF}$ = 32ms
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control.

## ■ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage on any pin relative to $V_{SS}$ | -1V to +7V |
| Operating temperature, Ta (Ambient) | 0°C to +70°C |
| Storage temperature | -55°C to +125°C |
| Short circuit output current | 50mA |
| Power dissipation | 1W |

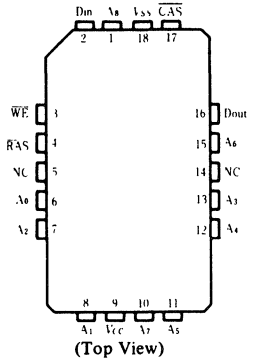
## ■PIN ARRANGEMENT

- HM51256LP Series




(Top View)

- HM51256LCP Series



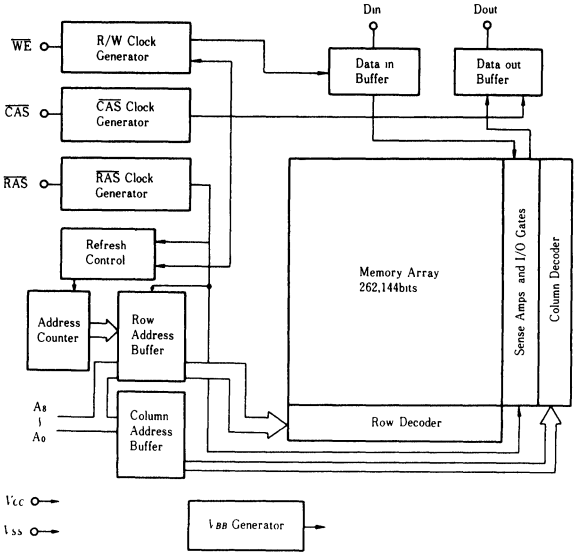

(Top View)

(Top View)

| | |
|---|---|
| $A_0$~$A_8$ | Address Inputs |
| $\overline{CAS}$ | Column Address Strobe |
| Din | Data In |
| Dout | Data Out |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{WE}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| $A_0$~$A_7$ | Refresh Address Inputs |

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

## ■BLOCK DIAGRAM




## ■RECOMMENDED DC OPERATING CONDITIONS ($Ta$=0 to +70°C)

| Parameter | Symbol | min | typ | max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input Low Voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note) 1. All voltages referenced to $V_{SS}$

## ■DC ELECTRICAL CHARACTERISTICS ($Ta$=0 to +70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V)

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}$=min) | $I_{CC1}$ | — | 60 | — | 50 | — | 40 | mA | 1 |
| Standby Current ($\overline{RAS}$=$V_{IH}$, Dout=High Impedance) | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | |
| Refresh Current ($\overline{RAS}$ only Refresh, $t_{RC}$=min) | $I_{CC3}$ | — | 60 | — | 50 | — | 40 | mA | |
| Standby Current ($\overline{RAS}$=$V_{IH}$, Dout Enable) | $I_{CC4}$ | — | 6 | — | 6 | — | 6 | mA | 1 |
| Standby Current ($\overline{RAS}$, $\overline{CAS}$=$V_{CC}$−0.2V) | $I_{CC5}$ | — | 200 | — | 200 | — | 200 | μA | |
| Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, $t_{RC}$=min) | $I_{CC6}$ | — | 55 | — | 45 | — | 35 | mA | |
| Page Mode Supply Current ($\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ Cycling, $t_{PC}$=min) | $I_{CC7}$ | — | 60 | — | 50 | — | 40 | mA | 1 |
| Input leakage (0≤$V_{in}$≤7V) | $I_{LI}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output leakage (0≤$V_{out}$≤7V, Dout=Disable) | $I_{LO}$ | −10 | 10 | −10 | 10 | −10 | 10 | μA | |
| Output levels High ($I_{out}$=−5mA) | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output levels Low ($I_{out}$=4.2mA) | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |

Notes) 1 $I_{CC}$ depends on output loading condition when the device is selected $I_{CC}$ max is specified at the output open condition

## ■CAPACITANCE ($V_{CC}$=5V±10%, $Ta$=25°C)

| Parameter | | Symbol | typ | max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input Capacitance | Address, Data-in | $C_{I1}$ | — | 5 | pF | 1 |
| | Clocks | $C_{I2}$ | — | 7 | | 1 |
| Output Capacitance | Data-out | $C_O$ | — | 7 | | 1, 2 |

Notes) 1 Capacitance measured with Boonton Meter or effective capacitance measuring method
2. $\overline{CAS}$=$V_{IH}$ to disable Dout

## ■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($Ta$=0 to +70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V)

### ● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 180 | – | 210 | – | 250 | – | ns | |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 70 | – | 80 | – | 90 | – | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 65 | 10000 | 75 | 10000 | 95 | 10000 | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 25 | – | 30 | – | 35 | – | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | – | 0 | – | 0 | – | ns | |
| Column Address Hold Time | $t_{CAH}$ | 20 | – | 25 | – | 30 | – | ns | |
| Column Address Hold Time to $\overline{RAS}$ | $t_{AR}$ | 75 | – | 90 | – | 110 | – | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 25 | 75 | 25 | 90 | 30 | 115 | ns | 8 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 20 | 55 | 20 | 65 | 25 | 80 | ns | 9 |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 25 | – | 30 | – | 35 | – | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 100 | – | 120 | – | 150 | – | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | – | 10 | – | 10 | – | ns | |
| Row Address Set-up Time | $t_{ASR}$ | 0 | – | 0 | – | 0 | – | ns | |
| Row Address Hold Time | $t_{RAH}$ | 15 | – | 15 | – | 20 | – | ns | |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 7 |
| Refresh Period | $t_{REF}$ | – | 4 | – | 4 | – | 4 | ms | |
| Refresh Period | $t_{REF2}$ | – | 32 | – | 32 | – | 32 | ms | 18 |

### ● Read Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | – | 100 | – | 120 | – | 150 | ns | 2, 3 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | – | 25 | – | 30 | – | 35 | ns | 3, 4 |
| Access Time from Address | $t_{AA}$ | – | 45 | – | 55 | – | 70 | ns | 3, 5, 14 |
| Read Command Set-up Time | $t_{RCS}$ | 0 | – | 0 | – | 0 | – | ns | |
| Read Command Hold Time to $\overline{CAS}$ | $t_{RCH}$ | 0 | – | 0 | – | 0 | – | ns | |
| Read Command Hold Time to $\overline{RAS}$ | $t_{RRH}$ | 10 | – | 10 | – | 10 | – | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 45 | – | 55 | – | 70 | – | ns | |
| Output Buffer Turn-off Time | $t_{OFF}$ | 0 | 25 | 0 | 30 | 0 | 35 | ns | 6 |

### ● Write Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | – | 0 | – | 0 | – | ns | 10 |
| Write Command Hold Time | $t_{WCH}$ | 25 | – | 30 | – | 35 | – | ns | |
| Write Command Hold Time to $\overline{RAS}$ | $t_{WCR}$ | 80 | – | 95 | – | 115 | – | ns | |
| Write Command Pulse Width | $t_{WP}$ | 20 | – | 25 | – | 30 | – | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 25 | – | 30 | – | 35 | – | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 25 | – | 30 | – | 35 | – | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | – | 0 | – | 0 | – | ns | 11 |
| Data-in Hold Time | $t_{DH}$ | 20 | – | 25 | – | 30 | – | ns | 10, 11 |
| Data-in Hold Time to $\overline{RAS}$ | $t_{DHR}$ | 75 | – | 90 | – | 110 | – | ns | |

### ● Read-Modify-Write Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| Read-Write Cycle Time | $t_{RWC}$ | 210 | – | 245 | – | 290 | – | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 100 | – | 120 | – | 150 | – | ns | 10 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 25 | – | 30 | – | 35 | – | ns | 10 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 45 | – | 55 | – | 70 | – | ns | 10 |

## ● Refresh Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CSR}$ | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CHR}$ | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time | $t_{RPC}$ | 15 | – | 15 | – | 15 | – | ns | |

## ● High Speed Page Mode Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| High Speed Page Mode Cycle Time | $t_{PC}$ | 55 | – | 65 | – | 80 | – | ns | 19, 21 |
| High Speed Page Mode $\overline{RAS}$ Pulse Width | $t_{RAPC}$ | 65 | 75000 | 75 | 75000 | 95 | 75000 | ns | 20 |
| $\overline{RAS}$ to Second $\overline{WE}$ Delay Time | $t_{RSW}$ | 105 | – | 125 | – | 155 | – | ns | |
| $\overline{CAS}$ Precharge Time | $t_{CP}$ | 15 | – | 20 | – | 20 | – | ns | |
| Write Invalid Time | $t_{WI}$ | 10 | – | 15 | – | 15 | – | ns | |
| Access Time from Column Precharge Time | $t_{CAP}$ | – | 50 | – | 60 | – | 75 | ns | 21 |

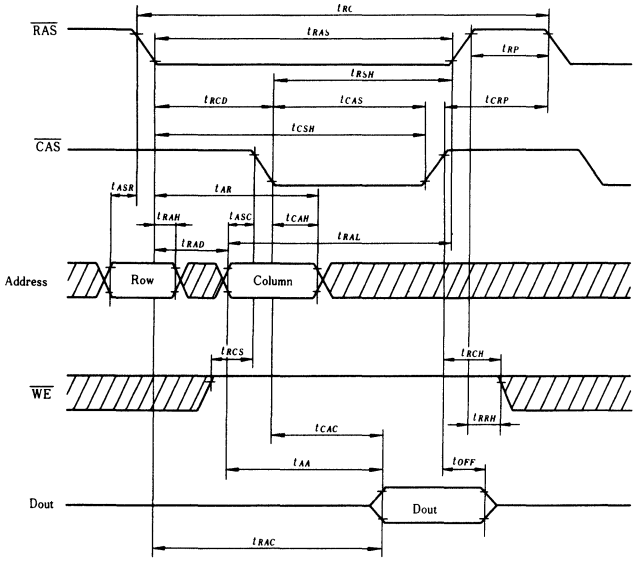
## ● High Speed Page Mode Read-Modify-Write Cycle

| Parameter | Symbol | HM5126LP/LCP-10 | | HM5126LP/LCP-12 | | HM5126LP/LCP-15 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| High Speed Page Mode Cycle Time on Read-Write | $t_{RWPC}$ | 95 | – | 115 | – | 145 | – | ns | 12 |
| Access Time from Previous $\overline{WE}$ | $t_{PWA}$ | – | 90 | – | 110 | – | 140 | ns | 3, 13 |
| Previous $\overline{WE}$ to Column Address Delay Time | $t_{WAD}$ | 25 | 45 | 30 | 55 | 35 | 70 | ns | 15 |

Notes:
1. AC measurements assume $t_T$ = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value show in this table, $t_{RAC}$ exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
8. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only, if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
9. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a Reference point only, if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
10. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read modify write cycles.
12. $t_{RWPC}$ (min) = $t_{AWD}$ (min) + $t_{WAD}$ (max) + $t_T$.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If $t_{WAD}$ is greater than the maximum recomended value shown in this table $t_{PWA}$ exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the $t_{WAD}$ (max) limit insures that $t_{PWA}$ (max) can be met, $t_{WAD}$ (max) is specified as a reference point only, if $t_{WAD}$ is greater than the specified $t_{WAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
16. An intial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
17. At least 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. The HM51256L extends the refresh period to 32ms during $\overline{RAS}$ only refresh operation.
19. Assumes that $t_{ASC} = t_{CP} - 5$ns.
20. $t_{RAPC}$ defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
21. Access time is determined by the longer of $t_{AA}$ or $t_{CAC}$ or $t_{CAP}$.

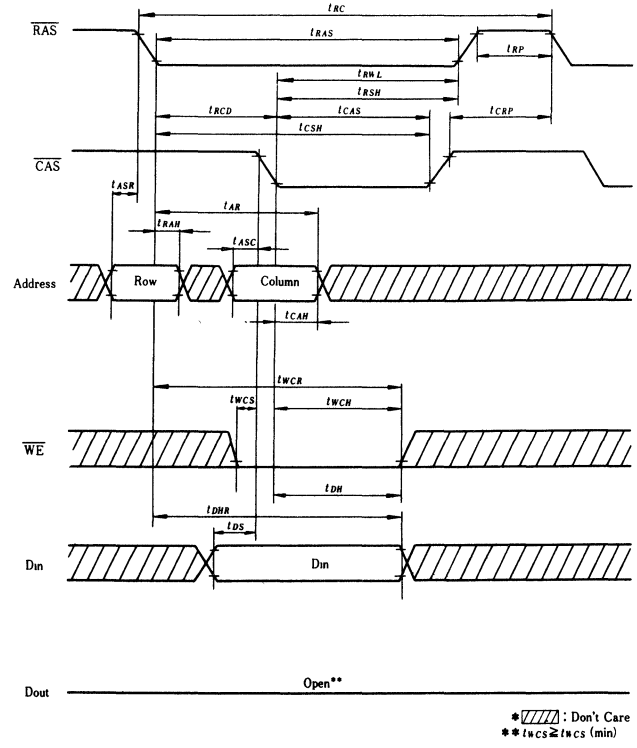
## ■TIMING WAVEFORMS

● Read Cycle



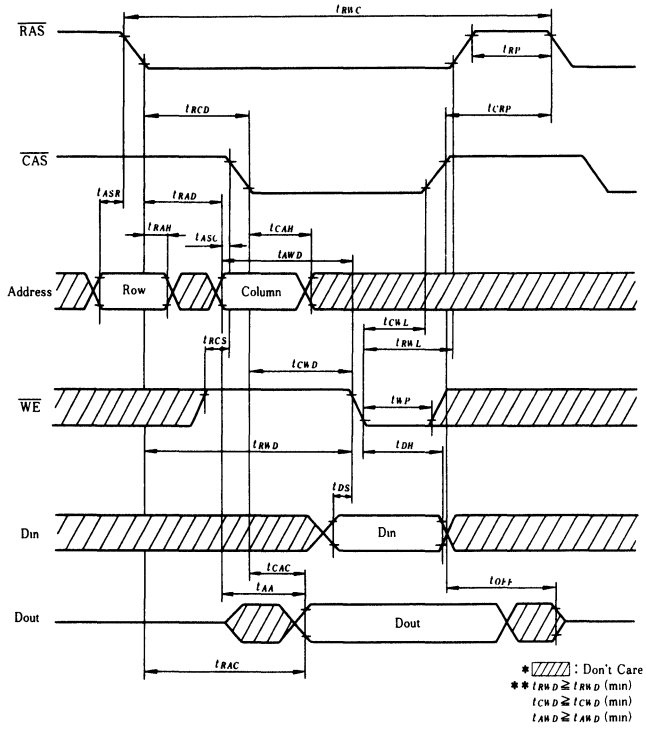

● Write Cycle

*▨: Don't Care

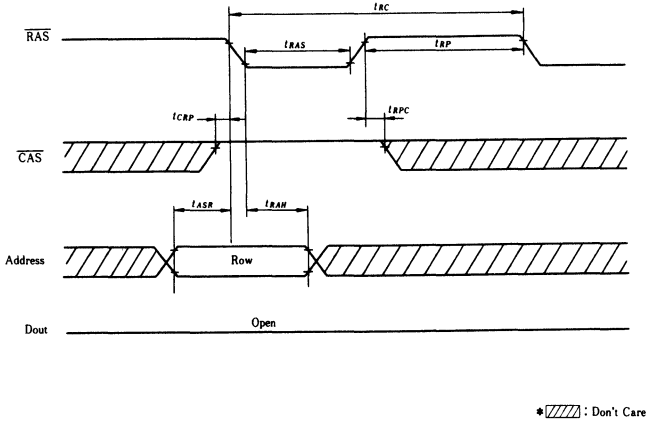



*▨: Don't Care
**$t_{WCS} \geq t_{WCS}$ (min)

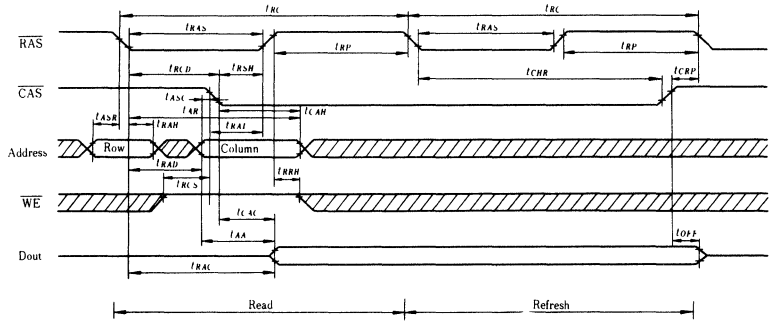
## ● Read Modify Write Cycle




## ● $\overline{\text{RAS}}$ Only Refresh Cycle

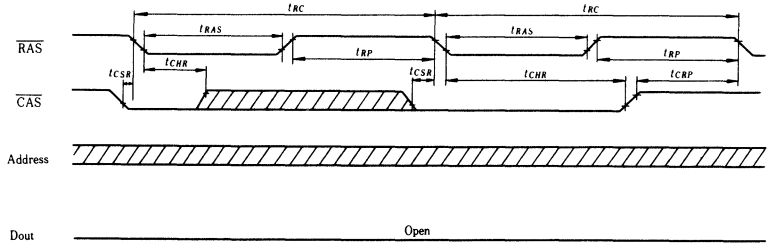


## ● Hidden Refresh Cycle



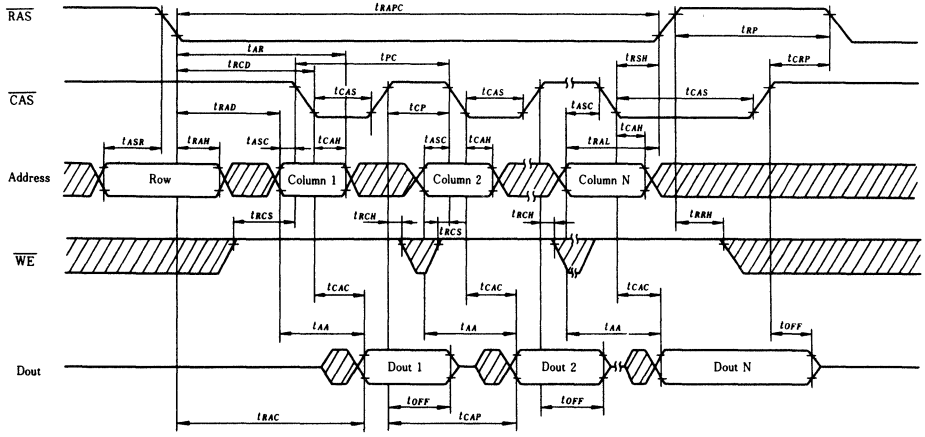

*▨ : Don't Care

## ● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



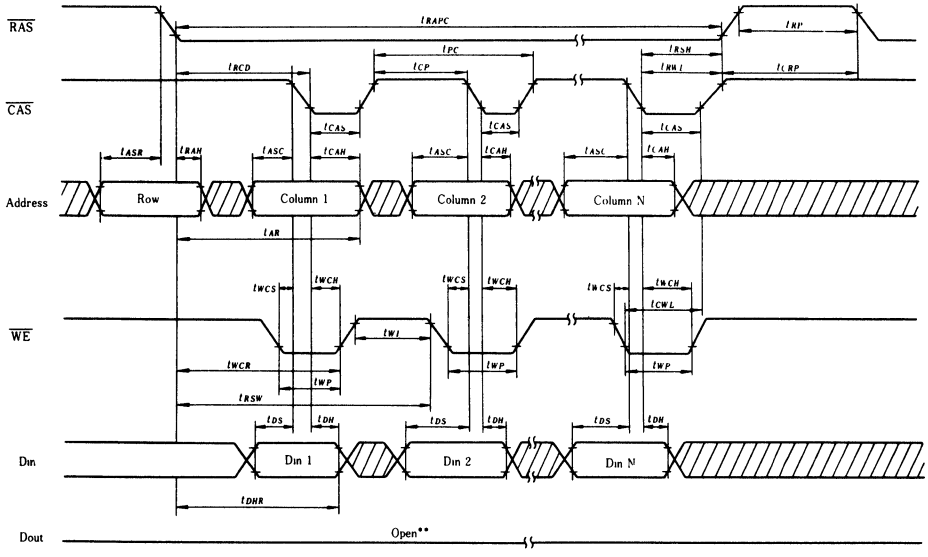

*▨ : Don't Care

## ● High Speed Page Mode Read Cycle



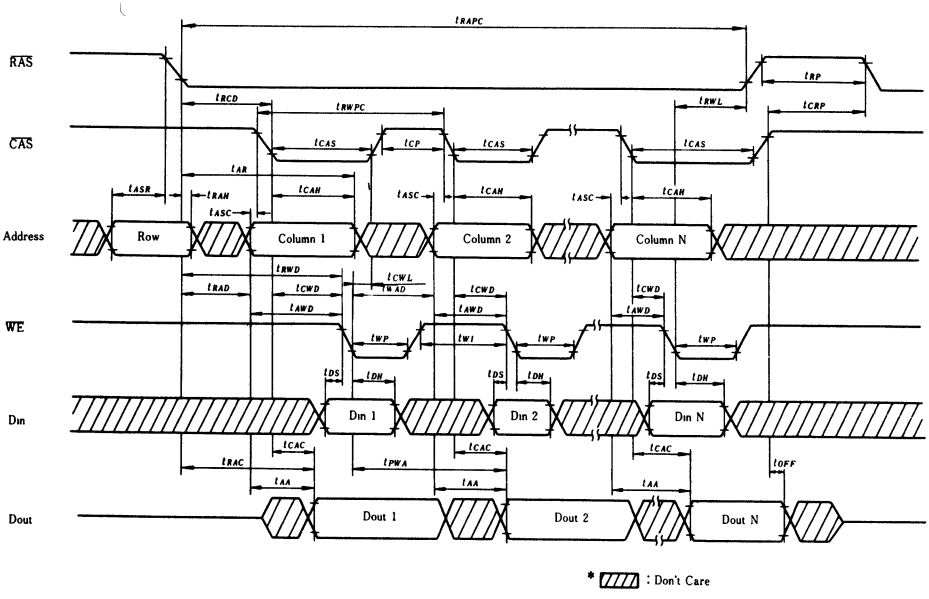

*▨ : Don't Care

## ● High Speed Page Mode Write Cycle




* ▨ : Don't Care
** $t_{WCS} \geq t_{WCS}$ (min)

## ● High Speed Page Mode Read Modify Write Cycle




* ▨ : Don't Care