



ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximumrated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."

TMS2332 4096-WORD BY 8-BIT READ-ONLY MEMORY

N PACKAGE

A7 1 U24 VCC

23 A8

22 🗌 A 9

21 A11

19 A10

17008

16007

15 06

14 05

13004

18 51/51

20 E/E/S2/S2

A6 2

A5 3

A4 4

A3 5

A216

A1 07

A0 18

Q1 []9

02010

03[11

VSS 12

SEPTEMBER 1984 - REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address TMS2332-15 150 ns TMS2332-20 200 ns TMS2332-25 250 ns
- Pin Compatible with 2732A EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation ... 330 mW
- Worst Case Standby Power Dissipation ... 82.5 mW

description

The TMS2332 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS2332 ideal for microprocessorbased systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

P	IN NOMENCLATURE
A0-A11	Address Inputs
Ē/E/S2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S1/S1	Chip Select
Vcc	5-V Supply
VSS	Ground

ROMs

7-3

The TMS2332 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 18 and 20 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 18 and 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mountinghole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 is the most-significant bit of the word address.

chip selects (S1 or S1 and S2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a lowlevel input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.



TMS2332 4096-WORD BY 8-BIT READ-ONLY MEMORY

chip enable/power down (E or E) or chip select (S2 or S2)

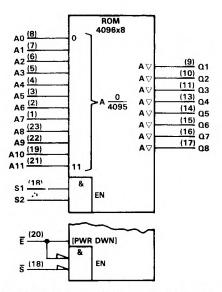
Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (\overline{E} or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. When pin 20 is programmed as a chip-select pin, it is functionally identical to pin 18.

data out (Q1-Q8)

The eight outputs must be enabled by pins 18 and 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]



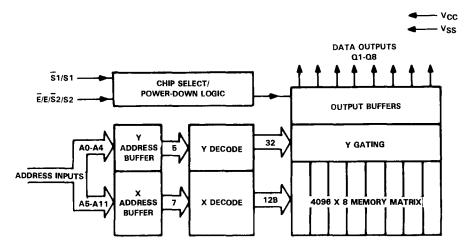


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pins 18 and 20 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select (\$2 or \$2) or a chip-enable/power-down (\$E or \$E) pin.



functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1)	–0.5 V to 7 ∨
Output voltage range (see Note 1)	. −1 V to 7 V
Input voltage range (see Note 1)	1 V to 7 V
Power dissipation	500 mW
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range	55°C to 150°C

NOTE 1: Voltage values are with respect to $\mathsf{V}_{SS}.$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2	. ``	CC+1	V
VIL	Low-level input voltege	-1		0.8	V
TA	Opereting free-air temperature	0		70	°C



TMS2332 4096-WORD BY 8-BIT READ-ONLY MEMORY

electrical characteristics, $T_A = 0^{\circ}C$ to 70°C, $V_{CC} = 5 V \pm 10\%$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MAX	UNIT
VOH	High-level output voltage	$V_{\rm CC} = 4.5 V,$	IOH = -1 mA	2.4		V
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	I _{OL} = 2.1 mA		0.4	V
4	Input current	V _{CC} = 5.5 V,	0 V ≤ VIN ≤ 5.5 V		10	μA
10	Output leakage current	$V_0 = 0.4 \text{ V to } V_{CC}$	Chip deselected		±10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	VI = VCC output not loaded		60	mA
ICC2	Supply current from V _{CC} (power down)	$V_{CC} = 5.5 V$			15	mA
Ci	Input capacitance	V _O = 0 V, f = 1 MHz	$T_{A} = 25^{\circ}C,$		6	ρF
Co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,		12	ρF

switching characteristics, T_A = 0°C to 70°C, V_{CC}, = 5 V \pm 10% (see Figure 1)[†]

		TMS2364-15		TMS2332-20		TMS2332-25		
	PARAMETER		MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)	Access time from address		150		200		250	ns
ta(S)	Access time from chip select		120		120		120	ns
ta(PD)	Access time from chip enable/power down		150		200		250	ns
t _{v(A)}	Output data valid after address change	0		0		0		ns
tdis	Output disable time from chip select/chip enable		100		100		100	ns

[†] All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

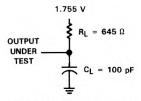
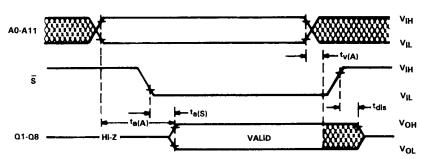


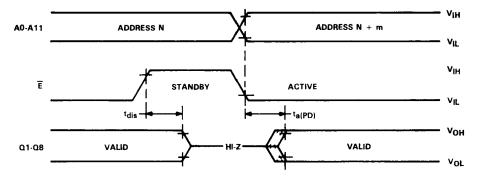
FIGURE 1. LOAD CIRCUIT



read cycle timing



standby mode





ROMs

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TMS2332 4096-WORD BY 8-BIT READ-ONLY MEMORY

PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2332 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

SPECIFICATION NUMB	ER:	
CUSTOMER IS AL	MBER/SYMBOLIZATION: LOWED TWO (2) LINES IC CHARACTERS PER LI	
ADDRESS ACCESS TIM	1E (SPEED):	
PACKAGE TYPE: PLAS	TIC (N)	
PIN OPTIONS: 1 = HIGH	I, 0=LOW, PD=POWER	R DOWN, CS = CHIP SELECT
PIN 18:	PIN 20:	PD/CS:



N PACKAGE

(TOP VIEW)

NC 1 U28 VCC

A1202

A7 3

A6 14

A5 5

A406

A3 7

A2 8

A1 9

A0 10

Q1 11

02 12

03 13

VSS 14

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27 NC/53/53

26 NC/S2/S2

25 A8

24 A9

23 A11

21 A10

19 Q8

17 06

16 05

15 04

22 S1/S1

20 E/E/S4/S4

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down TMS2364-15 150 ns TMS2364-20 200 ns TMS2364-25 250 ns
- Pin Compatible with 2764 EPROMs
- Worst Case Active Power Dissipation ... 330 mW
- Worst Case Standby Power Dissipation82.5 mW

description

The TMS2364 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. This makes the TMS2364 ideal for microprocessorbased systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS2364 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20, 22, 26, and 27 are mask programmable, providing additional

PIN	NOMENCLATURE
A0-A12	Address Inputs
E/E/S4/S4	Chip Enable/Power Down
	or Chip Select
NC	No Connection
Q1-Q8	Data Out
\$1/S1, \$2/S2,	Chip Selects
Š 3/S3	
Vcc	5-V Supply
VSS	Ground

system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22, 26, or 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mountinghole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (AO-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.



TMS2364 8192-WORD BY 8-BIT READ-ONLY MEMORY

chip selects (\$1 or \$1, \$2 or \$2, \$3 or \$3)

Pins 26 and 27 can be programmed during mask fabrication to be either chip selects or no connection (NC) at the inputs. Any pin(s) programmed as chip select(s) can also be programmed to be active with either a high- or a low-level input. If pins 26 and 27 are programmed as chip selects, and pins 20, 22, 26, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, 26, and 27 are not active, all eight outputs are in a high-impedance state. If pins 26 and 27 are programmed as no connection (NC), the previous discussion applies to the remaining active chip select(s).

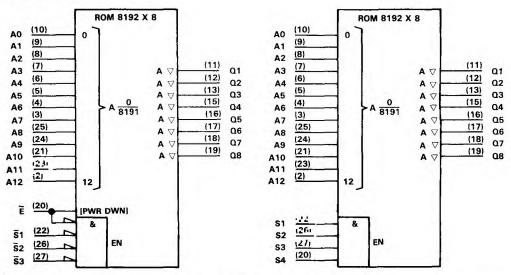
chip enable/power down (E or E) or chip select (S4 or S4)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (\overline{E} or E) or a fourth chip-select pin (\overline{S} 4 or S4). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 22, and pins 26 and 27 if programmed as chip selects, before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbols[†]

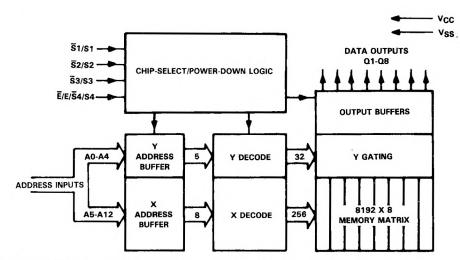


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pins 20 and 22, plus pins 26 and 27 if programmed as chip selects, can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a fourth chip select (\$4 or \$4) or a chip enable/power down (\$ or \$2).



functional block diagram[†]



[†] The diagram above assumes that pins 26 and 27 are programmed as chip selects.

absolute maximum ratings

Supply voltage range (see Note 1)	
Output voltage range (see Note 1)	
Input voltage range (see Note 1)	
Power dissipation	
Operating free-air temperature range	
Storage temperature range	

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	v
VIH	High-level input voltage	2	١	/CC+1	V
VIL	Low-level input voltage	-1		0.8	V
TA	Operating free-air temperature	0		70	°C



TMS2364 8192-WORD BY 8-BIT READ-ONLY MEMORY

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V \pm 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MAX	UNIT
VOH	High-level output voltage	V _{CC} = 4.5 V,	IOH = -1 mA	2.4		V
VOL	Low-level output voltage	V _{CC} = 4.5 V,	I _{OL} = 2.1 mA		0.4	v
4	Input current	VCC = 5.5 V,	$0 V \leq V_{IN} \leq 5.5 V$		10	μA
10	Output leakage current	$V_0 = 0.4 V$ to V_{CC} ,	Chip deselected		±10	μA
ICC1	Supply current from V _{CC} (active)	V _{CC} = 5.5 V,	VI = VCC output not loaded		60	mA
ICC2	Supply current from V _{CC} (power down)	V _{CC} = 5.5 V			15	mA
Ci	Input capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,		6	pF
co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_CC, = 5 V \pm 10% (see Figure 1[†])

		TMS2364-15	TMS2364-20	TMS2364-25	UNIT
	PARAMETER	MIN MAX	MIN MAX	MIN MAX	
ta(A)	Access time from address	150	200	250	
ta(S)	Access time from chip select	120	120	120	
ta(PD)	Access time from chip enable/power down	150	200	250	ns
tv(A)	Output data valid after address change	0	0	0	
tdis	Output disable time from chip select/chip enable	100	100	100	

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

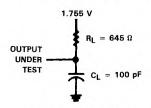
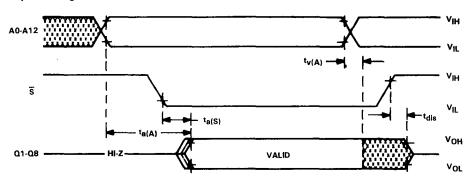


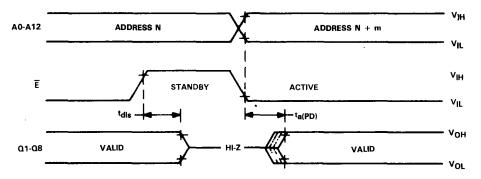
FIGURE 1. LOAD CIRCUIT



read cycle timing



standby mode





PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2364 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 32K or 64K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: SPECIFICATION NUMB ROM CODE NAME:	ER:	
	IBER/SYMBOLIZATION: LOWED TWO (2) LINES IC CHARACTERS PER L	S OF UP TO
ADDRESS ACCESS TIN	1E (SPEED):	
PACKAGE TYPE: PLAS	TIC (N)	
PIN OPTIONS: 1 = HIGH	I, 0=LOW, NC=NO CC	DNNECT, PD = POWER DOWN, CS = CHIP SELECT
PIN 20:	PIN 22:	PD/CS:
PIN 26:	PIN 27:	



ROMs

TMS4732 4096-WORD BY 8-BIT READ-ONLY MEMORY

MAY 1977 - REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address TMS4732-15 150 ns TMS4732-20 200 ns TMS4732-25 250 ns
- Pin-Compatible with TMS2532 EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation ... 330 mW
- Worst Case Standby Power Dissipation ... 82.5 mW

description

The TMS4732 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS4732 ideal for microprocessorbased systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS4732 is fully compatible with Series 74,

74S, or 74LS TTL and CMOS logic. The data

outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 21 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20 and 21.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mountinghole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (AO-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip selects (S1 or S1 and S2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a lowlevel input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

	N	PA	CH	AG	E		
	(1	rop	v	IEW	()		
A7	d	1	D	24	b	Vcc	
A6		2		23	6	A8	
A5		3		22	D	A9	
A4		4		21	b	S 1/S1	
A3		5		20	D.	E/E/S2/S	2
A2	D	6		19	Б	A10	
A1		7		18	6	A11	
AO		8		17	b.	0.8	
Q1		9		16	6	Q7	
02	D	10		15	6	Q6	
03		11		14	ħ.	Q5	
Vss	Ē	12		13	Б	Q4	

P	IN NOMENCLATURE
A0-A11	Address Inputs
Ē/E/S2/S2	Chip Enable/Power Down
	or Chip Select
Q1-Q8	Data Out
S1/S1	Chip Select
Vcc	5-V Supply
VSS	Ground

TMS4732 4096-Word by 8-bit read-only memory

chip enable/power down (\tilde{E} or E) or chip select ($\bar{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (\overline{E} or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With pin 20 programmed as a chip-select pin, it is functionally identical to pin 21.

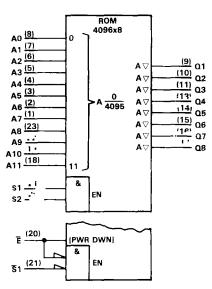
data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]

Λs

17:2

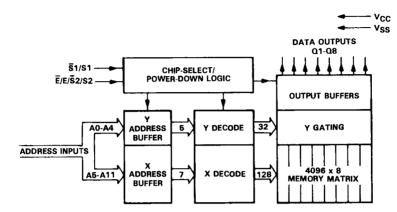


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pins 20 and 21 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select (\$2 or \$2) or a chip-enable/power-down (\$\vec{E}\$ or \$E) pin.



functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1)	-0.5 V to 7 V
Output voltage range (see Note 1)	. –1 V to 7 V
Input voltage range (see Note 1)	. –1 V to 7 V
Power dissipation	500 mW
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range	55°C to 150°C

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2	v	CC+1	V
ViL	Low-level input voltage	-1		0.8	V
TA	Operating free-air temperature	0		70	°C



TMS4732 4096-WORD BY 8-BIT READ-ONLY MEMORY

electrical characteristics, TA = 0°C to 70°C, VCC = 5 V \pm 10% (unless otherwise noted)

	PARAMETER	TES	T CONDITIONS	MIN	MAX	UNIT
Vон	High-level output voltage	$V_{\rm CC} = 4.5 V,$	loH = -1 mA	2.4		v
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	l _{OL} = 2.1 mA		0.4	v
łį –	Input current	$V_{CC} = 5.5 V,$	0 V ≤ VIN ≤ 5.5 V		10	μА
10	Output leakage current	$V_0 = 0.4 V$ to V_{CC} ,	Chip deselected		±10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	VI = VCC output not loaded		60	mA
ICC2	Supply current from V _{CC} (power down)	$V_{CC} = 5.5 V$			15	mA
Ci	Input capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,		6	pF
Co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	$T_{A} = 25^{\circ}C,$		12	p₽

switching characteristics, TA = 0°C to 70°C, VCC = 5 V \pm 10% (see Figure 1)[†]

		TMS4	732-15	TMS4	732-20	TMS4	732-25	UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)	Access time from address		150		200		250	ns
ta(S)	Access time from chip select		120		120		120	ns
ta(PD)	Access time from chip enable/power down		150		200		250	ns
tv(A)	Output data valid after address change	0		0		0		ns
tdis	Output disable time from chip select or chip enable		100		100		100	ns

[†] All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

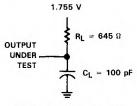
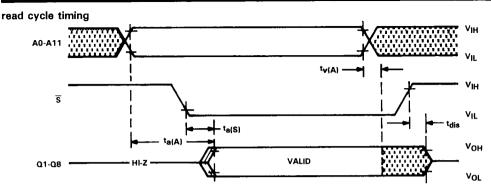
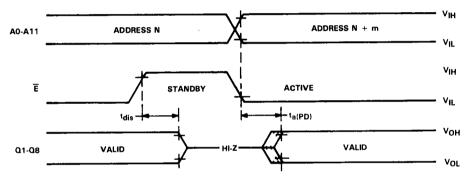


FIGURE 1. LOAD CIRCUIT





standby mode





TMS4732 4096-Word by 8-Bit read-only memory

PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4732 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER:		
SPECIFICATION NUMBER:		ROM CODE CHECKSUM:
CUSTOMER PART NUMBER/SY CUSTOMER IS ALLOWED 15 ALPHANUMERIC CHAR	MBOLIZATION: TWO (2) LINES OF UP T	
ADDRESS ACCESS TIME (SPE	ED):	
PACKAGE TYPE: PLASTIC (N)		
PIN OPTIONS: 1 = HIGH, 0 = LC	W, PD=POWER DOWN	I, CS = CHIP SELECT
PIN 20: PI	N 21: P	PD/CS:



TMS4764 8192-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1981 - REVISED NOVEMBER 1985

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Optional Power Down or Chip Select
- Single 5-V Power Supply
- Maximum Access Time from Address TMS4764-15 150 ns TMS4764-20 200 ns TMS4764-25 250 ns
- Worst Case Active Power Dissipation 330 mW
- Worst Case Standby Power Dissipation ... 82.5 mW

description

The TMS4764 is a 65,536-bit read-only memory organized as 8,192 words of 8-bit length. This makes the TMS4764 ideal for microprocessorbased systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS4764 is fully compatible with Series 74,

74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pin 20 is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pin 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mountinghole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (AO-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

chip enable/power down (E or E or chip select S or S)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (\overline{E} or E) or a chipselect pin (\overline{S} or S). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces ICC1, which in the active mode is 60 mA, to a standby current of 15 mA. When the signal on pin 20 is active, all eight outputs are enabled and the eight-bit addressed word can be read. When the signal is not active, all eight outputs are in a highimpedance state.



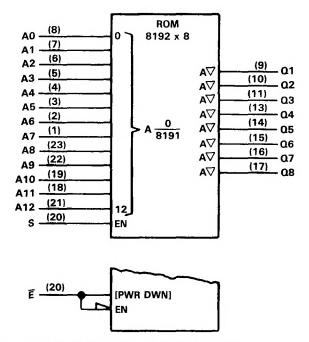
	N	PA	CK	A	SE		
	(1	TOP	v	IEV	V)		
A7	d	1	O	24	Ъ	Vcc	
A6		2		23	Б	A8	
A5		3		22	Þ	A9	
A4		4		21	Þ	A12	
A3		5		20	Þ	Ē/E/	S/S
A2		6		19	D	A10	
A1		7		18	6	A11	
AO		8		17	D	08	
Q1		9		16	D	07	
02		10		15	b	06	
03		11		14	b	Q5	
/ss	D	12		13	Б	Q4	

	PIN NOMENCLATURE
A0-A12	Address Inputs
E/E/S/S	Chip Enable/Power Down
	or Chip Select
01-08	Data Out
Vcc	5-V Supply
VSS	Ground

data out (Q1-Q8)

The eight outputs must be enabled by pin 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]

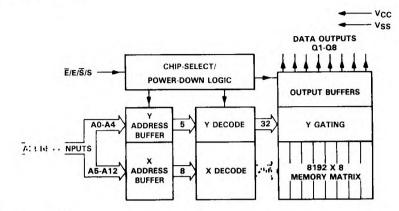


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin 20 can be active-high as shown in the upper symbol or active low as shown in the lower (partial) symbol. It can be either a chip select (\$ or \$) or a chip enable/power down (\$ or \$).



functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1)	-0.5 V to 7 V
Output voltage range (see Note 1)	-1 V to 7 V
Input voltage range (see Note 1)	-1 V to 7 V
Power dissipation	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature rangeE	55°C to 150°C

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage .	4.5	5	5.5	v
VIH	High-level input voltage	2	V	/CC+1	V
VIL	Low-level input voltage	-1		0.8	V
TA	Operating free-air temperature	0		70	°C

electrical characteristics, $T_A = 0$ °C to 70 °C, $V_{CC} = 5 V \pm 10\%$ (unless otherwise noted)

	PARAMETER	TES	T CONDITIONS	MIN	MAX	UNIT
VOH	High-level output voltage	$V_{CC} = 4.5 V,$	IOH = -1 mA	2.4		v
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	loL = 2.1 mA	1	0.4	v
ц	Input current	$V_{CC} = 5.5 V,$	$0 V \leq V_{IN} \leq 5.5 V$		10	μA
10	Output leakage current	$V_0 = 0.4 V$ to V_{CC} ,	Chip deselected		±10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	VI = VCC output not loaded		60	mA
ICC2	Supply current from VCC (power down)	V _{CC} = 5.5 V			15	mA
Ci	Input capacitance	V _O = 0 V, f = 1 MHz	$T_{A} = 25^{\circ}C,$		6	pF
C _o	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	$T_{A} = 25^{\circ}C,$		12	pF



TMS4764 8192-WORD BY 8-BIT READ-ONLY MEMORY

			TMS4764-15		TMS4764-20		TMS4764-25	
PARAMETER		PARAMETER MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)	Access time from address		150		200		250	
t _{a(S)}	Access time from chip select		120		120		120	
t _a (PD)	Access time from chip enable/power down		150		200		250	ns
tv(A)	Output data valid after address change	0		0		0		
^t dis	Output disable time from chip select or chip enable		100		100		100	1

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

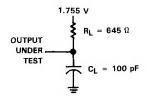


FIGURE 1. LOAD CIRCUIT

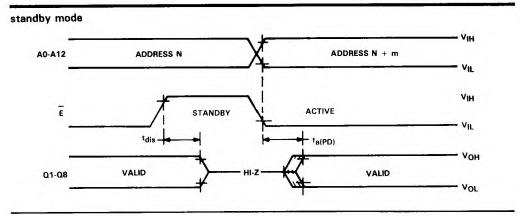
A0-A12 $\overline{E}/\overline{S}$ $\overline{U}(A)$ $\overline{U}(A)$

read cycle timing



ROMs 7

TMS4764 8192-WORD BY 8-BIT READ-ONLY MEMORY



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4764 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) Either 32K or 64K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER:	ROM CODE CHECKSUM:
CUSTOMER PART NUMBER/SYMBOLIZATION: CUSTOMER IS ALLOWED TWO (2) LINES OF U 15 ALPHANUMERIC CHARACTERS PER LINE	Р ТО
ADDRESS ACCESS TIME (SPEED):	
PACKAGE TYPE: PLASTIC (N)	
PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOW	/N, CS=CHIP SELECT
PIN 20: PD/CS:	



ROMs

ROMs 7

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JUNE 1983 - REVISEO NOVEMBER 1985

- 16,384 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down TMS47128-20 200 ns TMS47128-25 250 ns TMS47128-35 350 ns
- Pin Compatible with 27128 EPROMs
- Worst Case Active Power Dissipation ... 330 mW
- Worst Case Standby Power Dissipation ... 82.5 mW

description

The TMS47128 is a 131,072-bit read-only memory organized as 16,384 words of 8-bit length. This makes the TMS47128 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicongate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47128 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three-state for OR-tying multiple devices on a common bus. Pins 20, 22, and 27

N	PAC	KAGE	
(7	ГОР	VIEW)	
NC	ſι	J28	Vcc
A12	2	27	S2/S2
A7 🗌	3	26	A13
A6 🗋	4	25	A8
A5 🗋	5	24	A9
A4 🗋	6	23	A11
A3 🗌	7	22	<u></u>
A2 🗌	8	21	A10
A1 🗖	9	20	E/E/S3/S3
AO 🗋	10	19	Q8
Q1 [11	18	07
02 🖸	12	17	Q6
03 🗌	13	16	Q5
Vss C	14	15	Q4

PIN NOMENCLATURE						
A0-A13 Address Inputs						
Ē/E/S3/S3	Chip Enable/Power Down					
or Chip Select						
NC	No Connection					
Q1-QB	Data Out					
S1/S1, S2/S2 Chip Selects						
Vcc	5-V Supply					
V _{SS}	Ground					

4 ROMs

are mask-programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22 and 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mountinghole rows on 15,24 mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A13)

The address-valid interval determines the device cycle time. The 14-bit positive-logic address is decoded on chip to select one of 16,384 words of 8-bit length in the memory array. A0 is the least-significant bit and A13 is the most-significant bit of the word address.

chip select ($\overline{S}1$ or S1 and $\overline{S}2$ or S2)

Pins 22 and 27 can be programmed during mask fabrication to be active with either a high- or a low-level input. When the signals on pins 20, 22, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, and 27 are not active, all eight outputs are in a high-impedence state.

TMS47128 16,384-WORD BY 8-BIT READ-ONLY MEMORY

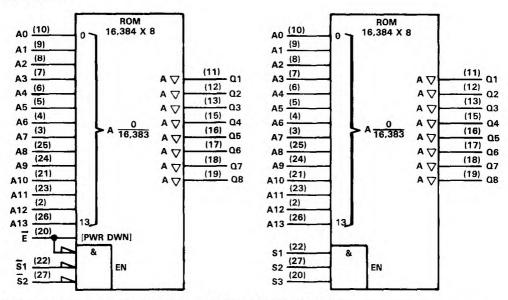
chip enable/power down (E or \tilde{E}) or chip select (S3 or $\overline{S3}$)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (E or \overline{E}) or a third chip-select pin (S3 or $\overline{S3}$). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1} , which in the active state is 60 mA, to a standby of I_{CC2} 15 mA. With the chip-select option, pin 20 is functionally identical to pins 22 and 27.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20, 22, and 27 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

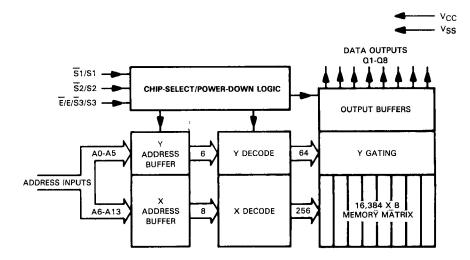
logic symbols[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pins 20, 22 and 27 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a third chip select (S3 or S3) or a chip enable/power down (E or E).



functional block diagram







TMS47128 16,384-WORD BY 8-BIT READ-ONLY MEMORY

absolute maximum ratings

Supply voltage range (see Note 1)	-0.5 V to 7 V
Output voltage range (see Note 1)	-1 V to 7 V
Input voltage range (see Note 1)	-1 V to 7 V
Power dissipation	
Operating free-air temperature range	0°C to 70°C
Storage temperature range5	5°C to 150°C

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2	Ĭ	/cc+1	V
VIL	Low-level input voltage	-1		0.8	V
TA	Operating free-air temperature	0		70	°C

electrical characteristics, TA = 0 °C to 70 °C, VCC = 5 V \pm 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MAX	UNIT
VOH	High-level output voltage	V _{CC} = 4.5 V,	IOH = -1 mA	2.4		v
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	I _{OL} = 2.1 mA		0.4	v
4	Input current	V _{CC} = 5.5 V,	0 V ≤ V _{IN} ≤ 5.5 V		10	μA
10	Output leakage current	$V_0 = 0.4 V$ to V_{CC} .	Chip deselected	1.1	±10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	VI = VCC output not loaded	1000	60	mA
ICC2	Supply current from V _{CC} (power down)	V _{CC} = 5.5 V			15	mA
Ci	Input capacitance	$V_0 = 0 V,$ f = 1 MHz	$T_{A} = 25^{\circ}C,$		6	pF
Co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	$T_A = 25^{\circ}C,$		12	pF

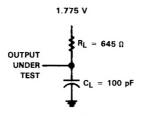
switching characteristics, TA = 0 °C to 70 °C, VCC = 5 V \pm 10% (see Figure 1) †

PARAMETER		TMS47	TMS47128-20		TMS47128-25		TMS47128-35	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)	Access time from address		200		250		350	
ta(S)	Access time from chip select		120	1000	120		150	
ta(PD)	Access time from power down/chip enable		200		250		350	ns
tv(A)	Output data valid after address change	0		0		0		
tdis	Output disable time from chip select/chip enable		100	1977	100		100	

[†]All AC measurements are made at 10% and 90% points.

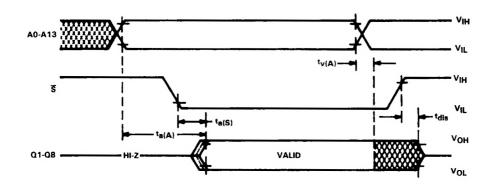


PARAMETER MEASUREMENT INFORMATION

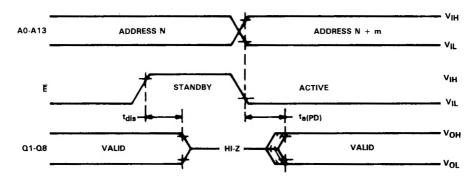




read cycle timing



standby mode





PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47128 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 16,384 8-bit words with address locations numbered 0 to 16,383. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A13 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (contact TI for details on card image transmission.) Either 64K or 128K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER:SPECIFICATION NUMBER: ROM CODE NAME:	
CUSTOMER PART NUMBER/SYMBOLIZATION: CUSTOMER IS ALLOWED TWO (2) LINES (15 ALPHANUMERIC CHARACTERS PER LIN	
ADDRESS ACCESS TIME (SPEED):	
PACKAGE TYPE: PLASTIC (N)	
PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER	DOWN, CS = CHIP SELECT
PIN 20: PIN 22:	PD/CS:
PIN 27:	



ROMs

TMS47256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1983 - REVISED NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down TMS47256-20 200 ns TMS47256-25 250 ns TMS47256-30 300 ns
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW
- Pin Compatible with 27256 and 27C256 Type EPROMs

description

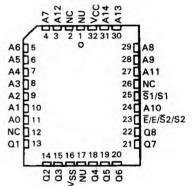
The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicongate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 22 (dual-in-line package) and pins 23 and 25 (chip carrier) are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of \overline{E} and \overline{S} pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package designed for surface mount applications using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

N	PAC	CKAG	E
C	гор	VIEW	n
	17	J28	Dvcc
A12	2	27	A14
A7 [3	26	A13
A6 🖸	4	25	D A8
A5 🖸	5	24	D A9
A4 🖸	6	23	A11
A3 🗖	7	22	S1/S1
A2	8	21	A10
A1	9	20	Ē/E/S2/S2
AO	10	19] 08
Q1 [11	18	107
02	12	17	106
03	13	16	ΠQ5
vss d	14	15	504





	PIN NOMENCLATURE					
A0-A14	Address Inputs					
E/E/S2/S2	Chip Enable/Power Down or Chip Select					
NC	No Connection					
NU	Make No External Connection					
Q1-Q8	Data Out					
S1/S1	Chip Select					
Vcc	5-V Supply					
VSS	Ground					

I'KODIICTION DATA documents contain information surrent as "disvibilication data. Products conform to specifications por the terms of Taxas Instruments standard warrenty. Production processing does not necessarily include testing of all parameters.



TMS47256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 is the most-significant bit of the word address.

chip select (S1 or S1)

Pin 22 (dual-in-line package) and pin 25 (chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both pins 22 and 20 (dual-in-line package) and pins 23 and 25 (chip carrier) are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When the signal on either of these pins is not active, all eight outputs are in a high-impedance state.

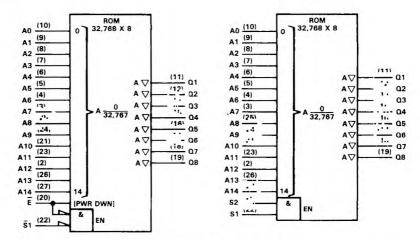
chip enable/power down (E or E) or chip select (S2 or S2)

Pin 20 (dual-in-line package) and pin 23 (chip carrier) can be programmed during mask fabrication to be a chip-enable/power down pin (\overline{E} or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22 for the dual-in-line package and pin 23 is functionally identical to pin 25 for the chip carrier.

data out (Q1-Q8)

The eight outputs must be enabled by the \overline{E} and \overline{S} pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbols[†]



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

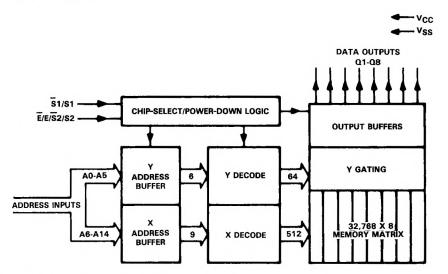
Pins 20 and 22 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a secondary chip select (S2 or \$2) or a chip enable/power down (E or E). The pin numbers shown are for the 28-pin dual-in-line package.



ROMs

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functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	v
Applied output voltage (see Note 1)1 V to 7	V
Applied input voltage (see Note 1)1 V to 7	v
Power dissipation	w
Operating free-air temperature range	°C
Storage temperature range	'n

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2		V _{CC} +1	V
VIL	Low-level input voltage	-1		0.8	v
TA	Operating free-air temperature	0		70	°C



TMS47256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

electrical characteristics, T_A = 0 °C to 70 °C, V_{CC} = 5 V \pm 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MAX	UNIT
VOH	High-level output voltage	$V_{\rm CC}=4.5~\rm V,$	loh = -1 mA	2.4		V
VOL	Low-level output voltage	$V_{CC} = 4.5 V_{,}$	$I_{OL} = 2.1 \text{ mA}$		0.4	V
h l	Input current	$V_{CC} = 5.5 V_{,}$	$0 V \leq V_{\rm IN} \leq 5.5 V$		10	μA
10	Output leakage current	$V_0 = 0 V$ to V_{CC} ,	Chip deselected	T	±10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	VI = VCC Output not loaded		60	mA
ICC2	Supply current from V _{CC} (power down)	V _{CC} = 5.5 V			15	mA
Ci	Input capacitance	V ₀ = 0 V, f = 1 MHz	$T_{A} = 25^{\circ}C,$		6	pF
Co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,		12	pF

switching characteristics, T_A = 0 °C to 70 °C, V_{CC} = 5 V \pm 10% (see Figure 1)[†]

PARAMETER		TMS47256-20		TMS47256-25		TMS47256-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MA	UNIT
ta(AD)	Access time from address		200		250			
ta(S)	Access time from chip select	1.	120		120	1	· · ·	6.00
ta(PD)	Access time from power down/chip enable		200		250		1.62.6	ns
tv(A)	Output data valid after address change	0	and the second	0		0		
tdis	Output disable time from chip select/chip enable			(i i i i i i i i i i i i i i i i i i i	100		_ · _	

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

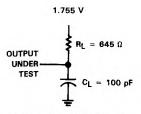
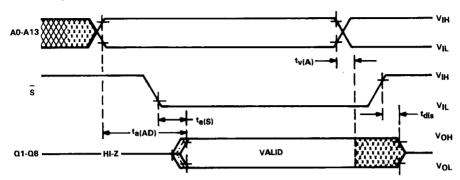


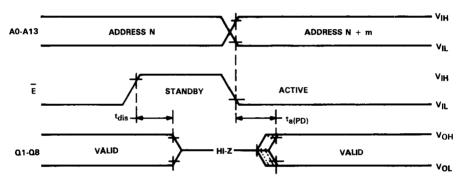
FIGURE 1. LOAD CIRCUIT



read cycle timing



standby mode





TMS47256 32,768-Word by 8-bit read-only memory

PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47256 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number from 00 and FF. Q1 is considered the least-significant bit and Q8 is the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _ SPECIFICATION ROM CODE NA	NUMBER:			CODE CH	ECKSUM:	
	RT NUMBER/S R IS ALLOWEI NUMERIC CHA	TWO (2) LIN	IES OF UP TO			_
ADDRESS ACC	ESS TIME (SPE	ED):				
PACKAGE TYP	E: PLASTIC (N)	s	URFACE MOUNT	(FM)		
PIN OPTIONS:	1 = HIGH,	0 =LOW,	PD = POWER D	OWN,	CS = CHIP SELECT	
N PACKAGE:	PIN 20	PIN	22	PD/CS_		
FM PACKAGE:	PIN 23	PIN	25	PD/CS_		



ADVANCE INFORMATION

TMS47C256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- HVCMOS Technology
- Maximum Access Time from Address or Power Down TMS47C256-15 150 ns TMS47C256-20 200 ns
 - TMS47C256-25 250 ns
- Pin Compatible with 27256 EPROMs
- Worst Case Active Power Dissipation . . . 275 mW
- Worst Case Standby Power Dissipation . . . 2.8 mW

description

The TMS47C256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47C256 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select pin(s).

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

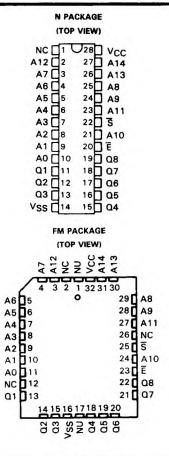
operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on-chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most-significant bit of the word address.

A: «A+u, i INFORMATION documents contain """""" on new products in the sampling or """" and "", """ on phase of development. Characteristic Jate a.:: "ther specifications are subject to change without notice.





PIN NOMENCLATURE				
A0-A14	Address Inputs			
Ē	Chip Enable/Power Down			
NC	No Connection			
NU	Make No External Connection			
01-08	Data Out			
5	Chip Select			
Vcc	5-V Supply			
VSS	Ground			

TMS47C256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

chip select (S)

When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on either the chip-select or the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state.

chip enable/power down (E)

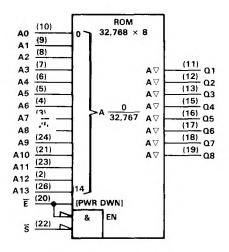
When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1} , which in the active state is 50 mA, to a standby I_{CC2} of 500 μ A. In this mode all outputs are in a high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]

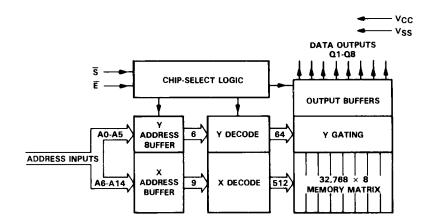




[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The pin numbers shown are for the 28-pin dual-in-line package.



functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	. –0.5 V to 7 V
Applied output voltage (see Note 1)0.3 V to	VCC + 0.3 V
Applied input voltage (see Note 1)0.3 V to	VCC + 0.3 V
Power dissipation	300 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range5	55°C to 150°C

NOTE 1: Voltage values are with raspact to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	v
VIH	High-level input voltage	2		Vcc	v
VIL	Low-level input voltage	-0.5		0.8	v
TA	Operating free-air temperature	0		70	°C



TMS47C256 32,768-WORD BY 8-BIT READ-ONLY MEMORY

electrical characteristics, T_A = 0 °C to 70 °C, V_{CC} = 5 V \pm 10% (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN MAX	UNIT
VOH	High-level output voltage	$V_{CC} = 4.5 V,$	IOH = -400 μA	2.4	V
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	$I_{OL} = 2.1 \text{ mA}$	0.4	V
4	Input current	$V_{CC} = 5.5 V,$	0 V ≤ V _{IN} ≤ 5.5 V	10	μA
10	Output leakage current	$V_0 = 0 V$ to V_{CC} .	Chip deselected	± 10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V_{,}$	VI = VCC Output not loaded	50	mA
ICC2	Supply current from VCC (power down)	$V_{CC} = 5.5 V$		500	μA
Ci	Input capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,	6	pF
Co	Output capacitance	$V_0 = 0 V,$ f = 1 MHz	T _A = 25°C,	12	pF

switching characteristics, TA = 0 °C to 70 °C, VCC = 5 V \pm 10% (see Figure 1)[†]

PARAMETER		TMS470	256-15	TMS47	256-20	TMS470	256-25	UNIT
		MIN	MAX	MIN	MAX	MIN	MAT	UNE
ta(A)	Access time from address	Г	150	1	200		250	
ta(S)	Access time from chip select		75		75	1.1	100	
ta(PD)	Access time from power down/chip enable		150		200		250	ns
tv(A)	Output data valid after address change	0		0		0		
tdis	Output disable time from chip select/chip enable		60		60		60	

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

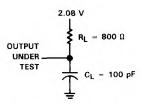
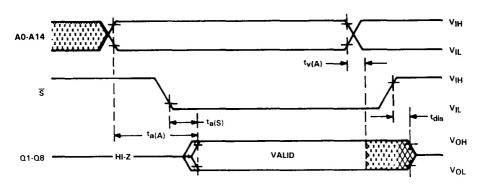


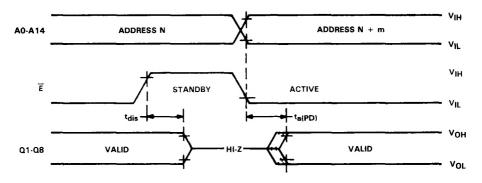
FIGURE 1. LOAD CIRCUIT



read cycle timing



standby mode





PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C256 is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMs can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

	ROM CODE CHECKSUM:
CUSTOMER PART NUMBER/SYMBOLIZATION: CUSTOMER IS ALLOWED TWO (2) LINES OF UF 15 ALPHANUMERIC CHARACTERS PER LINE	•то
ADDRESS ACCESS TIME (SPEED):	
PACKAGE TYPE: PLASTIC (N) SURFACE	MOUNT (FM)

ADVANCE INFORMATION

TMS47C512 65,536-WORD BY 8-BIT READ-ONLY MEMORY

A

A

1

NOVEMBER 1985

- 65,536 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL and CMOS Compatible
- Single 5-V Power Supply
- Standby Mode for Minimum Power Usage
- Maximum Access Time from Address or Power Down TMS47C512-20 200 ns TMS47C512-25 250 ns TMS47C512-30 300 ns
- Pin Compatible with 27512 EPROMs

description

The TMS47C512 is a 524,288-bit read-only memory organized as 65,536 words of 8-bit length. This makes the TMS47C512 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C512 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-select and chip-enable/power-down pins are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select and chipenable/power-down pins.

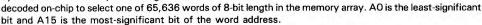
This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A15)

The address-valid interval determines the device

cycle time. The 16-bit positive-logic address is

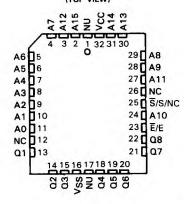


ADVANCE INFORMATION documents contain unitation of the about the sampling of properties of the sampling of the sa



		CKAG VIEW	
15	17	J28	JVcc
12	2	27	A14
A7 [3	26	A13
A6	4	25	A8
A5 🗌	5	24	A9
	6	23]A11
АЗС	7	22	S/S/NC
A2C	8	21]A10
A1C	9	20	Ē/E
AOC	10	19	08
	11	18] 07
02 Ē	12	17	06
aзĒ	13	16] Q5
ssE	14	15	04

TOP VIEW)



PIN NOMENCLATURE				
A0-A15	Address Inputs			
Ē/E	Chip Enable/Power Down			
NC	No Connection			
NU	Make No External Connection			
01-08	Data Out			
S/S	Chip Select			
Vcc	5-V Supply			
VSS	Ground			



TMS47C512 65,536-Word by 8-bit read-only memory

chip select (S or S)

The chip-select pin (pin 23 for the dual-in-line package and pin 25 for the chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signals on the chip-select and chip-enable/power-down pins are not active, all eight outputs are in a high-impedance state. Pin 22 (dual-in-line package) and pin 25 (chip carrier) can also be programmed as a no connection if only a chip enable is required.

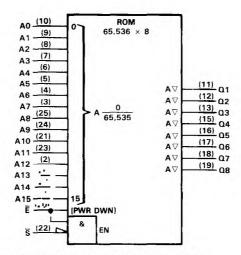
chip enable/power down (E)

The chip-enable/power-down pin (pin 20 for the dual-in-line package and pin 23 for the chip carrier) can be programmed during mask fabrication to be active with either a high-level or low-level input. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. In this mode all outputs are in the high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]

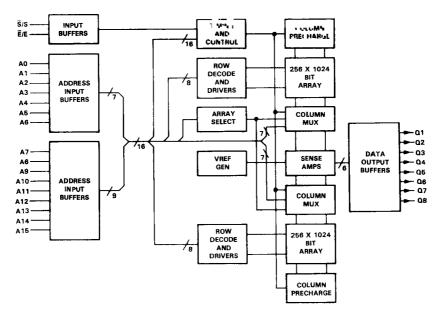


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The pin numbers shown are for the 28-pin dual-in-line package. Pins 20 and 22 can be active low as shown in the symbol above or active high. In addition, pin 22 can be a no connection.



functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	-0.5 V to 7 V
Applied output voltage (see Note 1)0.3 V to	
Applied input voltage (see Note 1)0.3 V to	V _{CC} + 0.3 V
Power dissipation	T. B.D.
Operating free-air temperature range	0°C to 70°C
Storage temperature range	5°C to 150°C

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

1		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2	•	v _c c	V
VIL	Low-level input voitage	-0.5		0.8	V
TA	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.



TMS47C512 65,536-WORD BY 8-BIT READ-ONLY MEMORY

PARAMETER		TE	MIN MAX	UNIT	
VOH	High-level output voltage	$V_{CC} = 4.5 V,$	IOH = -400 μA	2.4	V
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	IOL = 2.1 mA	0.4	v
4	Input leakage current	$V_{CC} = 5.5 V,$	0 V ≤ VIN ≤ 5.5 V	10	μA
ю	Output leakage current	$V_0 = 0 V to V_{CC}$	Chip deselected	±10	μA
ICC1	Supply current from V _{CC} (active)	V _{CC} = 5.5 V,	VI = VCC Output not loaded	T.B.D.	
ICC2	Supply current from VCC (standby)	V _{CC} = 5.5 V		T.B.D.	
Ci	Input capacitance	$V_0 = 0 V,$ f = 1 MHz	$T_A = 25 ^{\circ}C,$	10	pF
co	Output capacitance	$V_0 = 0 V,$ t = 1 MHz	T _A = 25°C,	15	pF

electrical characteristics, $T_A = 0$ °C to 70 °C, $V_{CC} = 5 V \pm 10\%$ (unless otherwise noted)

switching characteristics, T_A = 0 °C to 70 °C, V_{CC} = 5 V \pm 10% (unless otherwise noted)

PARAMETER		TMS47C512-20		TMS47C512-25		TMS47C512-30		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ta(A)	Access time from address		200		250		300	
ta(S)	Access time from chip select		100		100		100	
ta(PD)	Access time from power down/chip enable		200		250	1000	300	ns
V(A)	Output data valid after address change	0		0		0		
tdis	Output disable time from chip select		100	1	100		100	

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

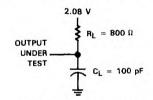
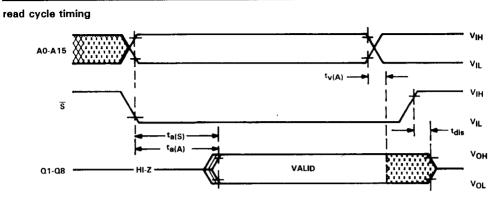


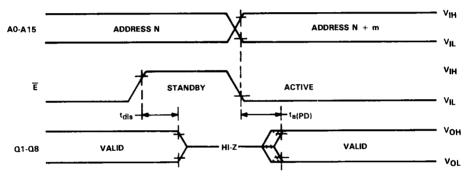
FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

7



standby mode





PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C512 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code requirements. The device is organized as 65,536 8-bit words with address locations numbered 0 to 65,535. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A15 is the most significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, or 512K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER:SPECIFICATION NUMBER:ROM CODE NAME:	
CUSTOMER PART NUMBER/SYMBOLIZATION: CUSTOMER IS ALLOWED TWO (2) LINES OF U 15 ALPHANUMERIC CHARACTERS PER LINE	Р ТО
ADDRESS ACCESS TIME (SPEED):	
PACKAGE TYPE: PLASTIC (N) SURFAC	E MOUNT (FM)
PIN OPTIONS: 1=HIGH, 0=LOW.	
N PACKAGE: PIN 20: PLCC: PIN 23:	PIN 22: PIN 25

ADVANCE INFORMATION

TMS47C1024 131,072-WORD BY 8-BIT READ-ONLY MEMORY

1

1

NOVEMBER 1985

- 131,072 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL and CMOS Compatible
- Single 5-V Power Supply
- Standby Mode for Minimum Power Usage
- Maximum Access Time from Address or Power Down TMS47C1024-20 200 ns TMS47C1024-25 250 ns TMS47C1024-30 300 ns

description

The TMS47C1024 is a 1,048,576-bit read-only memory organized as 131,072 words of 8-bit length. This makes the TMS47C1024 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C1024 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chipenable/power-down pin is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-enable/power-down pin.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A16)

The address-valid interval determines the device cycle time. The 17-bit positive-logic address is decoded on-chip to select one of 131,072 words of 8-bit length in the memory array. A0 is the least-significant bit and A16 is the most-significant bit of the word address.

٩	PA	CKAG	E
	TOP	VIEW)
A15 [n C	J28	Vcc
A12 C	2	27	A14
A7 C	3	26	A13
A6 C	4	25] AB
A5 C	5	24	A9
A4 C	6	23	JA11
A3 C	7	22	A16
A2	8	21	A10
A1	9	20]Ē/E
AOC	10	19	308
Q1 [11	18] 07
Q2 [12	17] Q6
03	13	16	05
Vss C	14	15	3~4

FM PACKAGE (TOP VIEW)

	100		24 F 24 A 32 31 30	Û.
AG	15	0	29	A8
A5	6		28	A9
A4	7		27	A11
A3	8		26	A16
A2] 9		25	NC
A1	10		24	A10
AO	111		23	Ē/E
NC	12		22	08
01	13		21	07
	141	51617	181920	

PIN NOMENCLATURE				
A0-A16	Address Inputs			
Ē/E	Chip Enable/Power Down			
NC	No Connection			
NU	Make No Internal Connection			
Q1-Q8	Data Out			
Vcc	5-V Supply			
VSS	Ground			

ADVANCE INFORMATION documents contain information on new protects in the sampling or preproduction phase of levers; ment. Characteristic data and other specifics:...s are subject to change without notice.



ROMs

TMS47C1024 131,072-WORD BY 8-BIT READ-ONLY MEMORY

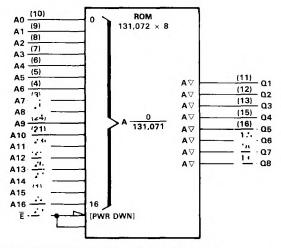
chip-enable/power down (E or E)

The chip-enable/power-down pin can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on the chip-enable/power-down pin is active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state and the device goes into a standby current mode.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-enable/power-down pin before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol[†]

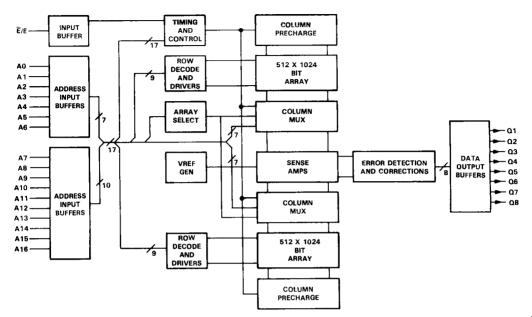


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The pin numbers shown are for the 28-pin dual-in-line package. Pin 20 can be active low as shown in the symbol above or active high.



functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	–0.5 V to 7 V
Applied output voltage (see Note 1)0.3 V to	VCC + 0.3 V
Applied input voltage (see Note 1)0.3 V to	V _{CC} + 0.3 V
Power dissipation	T.B.D.
Operating free-air temperature range	0°C to 70°C
Storage temperature range	55°C to 150°C

NOTE 1: Voltage values are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltaga	4.5	5	5.5	V
VIH	High-level input voltage	2		∨ c c	V
VIL	Low-level input voltage	-0.5		0.8	V
TA	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.



TMS47C1024 131,072-Word by 8-bit read-only memory

PARAMETER		TES	TEST CONDITIONS			UNIT
VOH.	High-level output voltage	$V_{CC} = 4.5 V,$	l _{OH} ≃ −400 µA	2.4		v
VOL	Low-level output voltage	$V_{CC} = 4.5 V,$	IOL = 2.1 mA		0.4	v
4	Input leakage currant	$V_{CC} = 5.5 V,$	0 V ≤ VIN ≤ 5.5 V		±10	μA
10	Output leakage current	$V_0 = 0.4 V \text{ to } V_{CC}$	Chip deselected		± 10	μA
ICC1	Supply current from V _{CC} (active)	$V_{CC} = 5.5 V,$	V ₁ = V _{CC} Output not loaded	T	T.B.D.	
ICC2	Supply current from V _{CC} (standby)	$V_{CC} = 5.5 V$			T.B.D.	
ci	Input capacitance	$V_0 = 0 V$,	$T_{A} = 25 ^{\circ}C,$		10	- 5
		f = 1 MHz			10	pF
Co	Output capacitance	$V_0 = 0 V$	$T_{A} = 25 ^{\circ}C,$		15	
		f = 1 MHz			15	pF

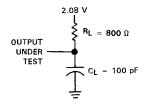
electrical characteristics, TA = 0 °C to 70 °C, VCC = 5 V \pm 10% (unless otherwise noted)

switching characteristics, TA = 0 °C to 70 °C, VCC = 5 V \pm 10% (see Figure 1) †

	PARAMETER		MS47C1024-20 TMS47C10			-25 TMS47C1024-30		
			MAX	MIN MAX		MIN	MAX	
ta(A)	Access time from address		200		250		300	
t _{a(E)}	Access time from chip enable				250		300	
tv(A)	Output data valid after address change	0		0		0		ńs
tdis	Output disable time from chip enable		100		100		100	

[†]All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

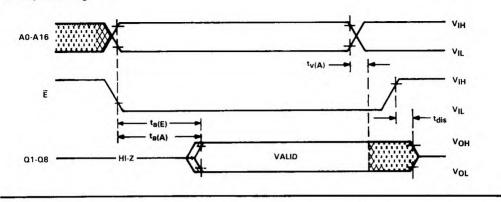




Additional information on these products can be obtained from the factory as it becomes available.



read cycle timing



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C1024 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 131,072 8-bit words with address locations numbered 0 to 131,071. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A16 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, 512K, or 1024K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER:	
SPECIFICATION NUMBER:	ROM CODE CHECKSUM:
CUSTOMER PART NUMBER/SYMBOLIZATION: CUSTOMER IS ALLOWED TWO (2) LINES OF U 15 ALPHANUMERIC CHARACTERS PER LINE	JP TO
ADDRESS ACCESS TIME (SPEED):	
PACKAGE TYPE: PLASTIC (N) SURF	ACE MOUNT (FM)
PIN OPTIONS: 1 = HIGH, 0 = LOW	
N PACKAGE: PIN 20: PLCC: PIN 23	



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ROMs

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