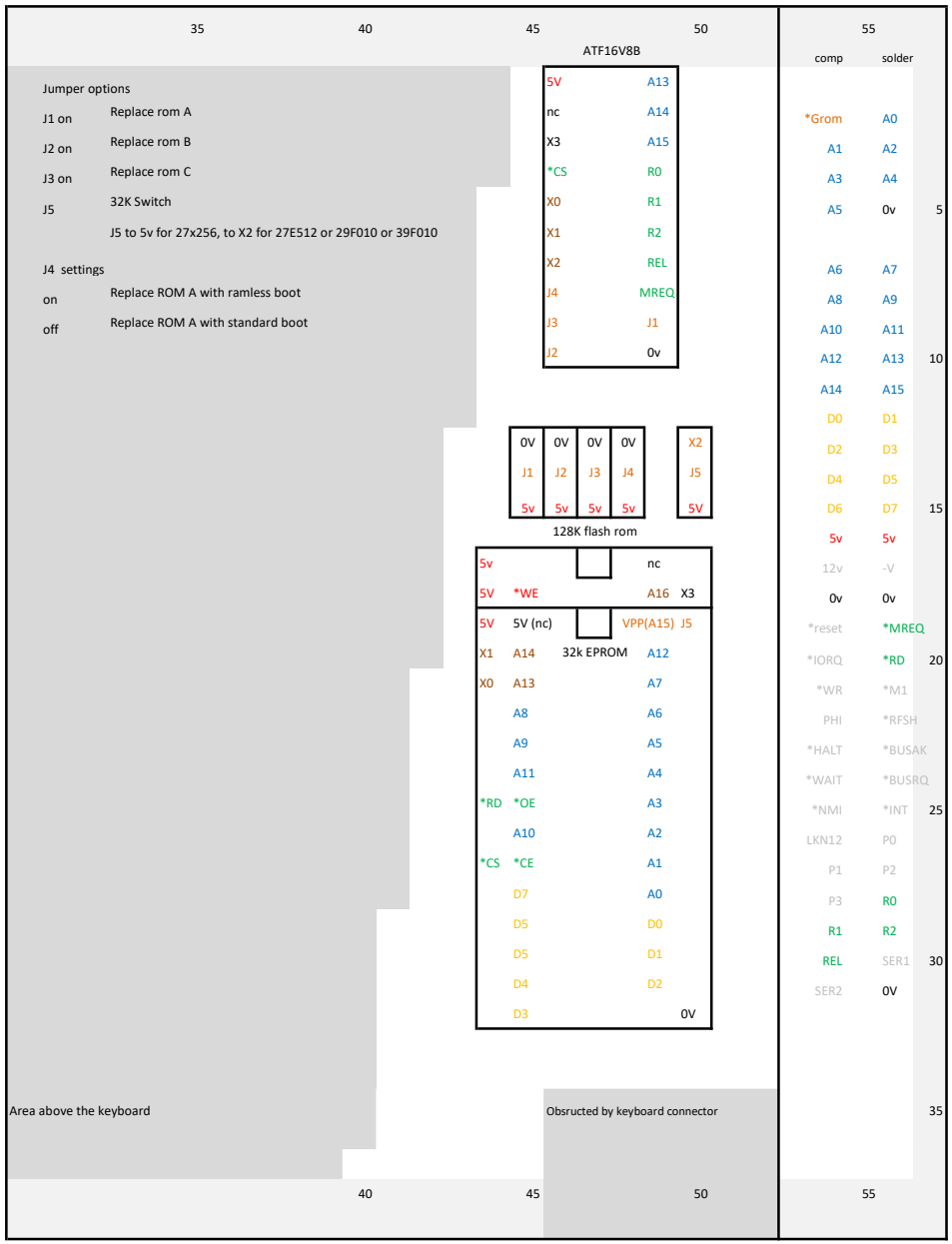

Rom Images	FLASH/EPROM address				CPU address
	X0	X1	X2	X3	
ROM A	0	0	0	0	first 8k all pages
ROM B	1	0	0	0	2nd 8k page 0
ROM C	0	1	0	0	2nd 8k page 1
RAMLESS	1	1	0	0	first 8k all pages

	J1	J2	J3	J4	A15	A14	A13	REL	R0	R1	R2
Page in ROM A	1	x	x	0	0	0	0	0	x	x	x
Page in ROM B	x	1	x	x	0	0	1	0	1	0	0
Page in ROM C	x	x	1	x	0	0	1	0	0	0	0
Page in RAMLESS A	1	x	x	1	0	0	0	0	x	x	x

CPLD driven X2 and X3 alows room for additional images in 64k+ devices