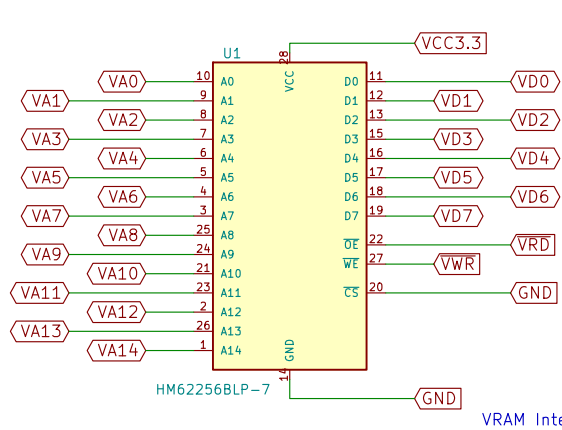
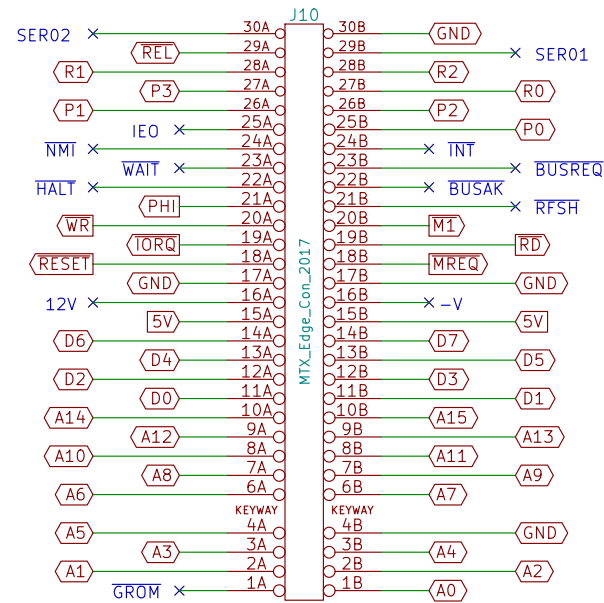
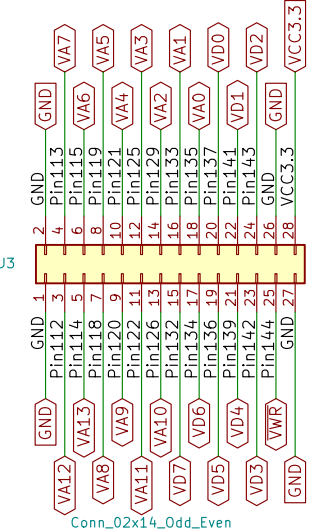


Using Board Edge Connector Footprint



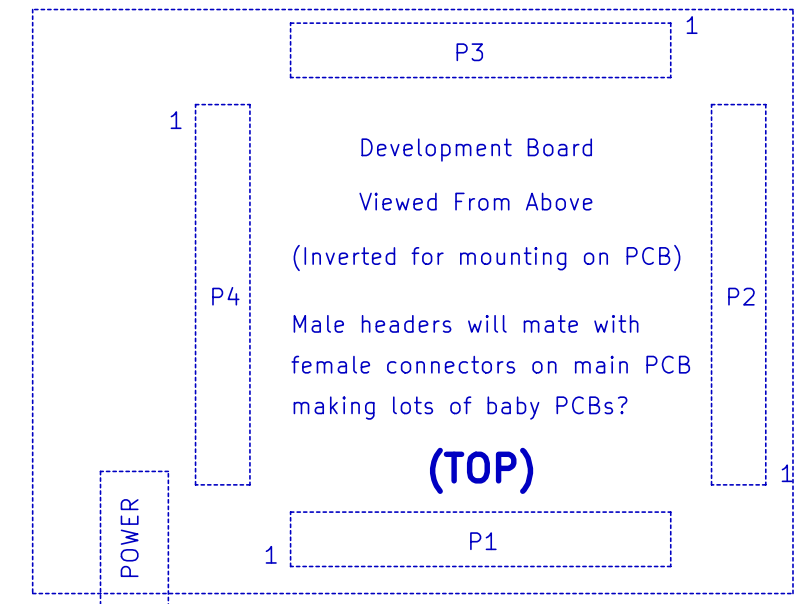
VRAM Interface
 Dlx are Inputs TO the MTX FROM the FPGA (3v to 5v)
 DOx are Outputs FROM the MTX TO the FPGA (5v to 3v)



NOTES

Change Log

- Ver 0.1 : Initial schematic based on prototype development
- Ver 0.2 : Changes for possible Speculator addition
 MREQ on J0/J10 to one of the spare LVC244 input (pin 8)
 3v downshifted MREQ LVC244 (pin 12) to pin 21 on the P4 FPGA header
 Pin 24 on the P4 FPGA header to A14 on the VRAM
 Also removed HD15 VGA connector
 Deleted 1.2v connections from FPGA board (J4 Pins 19 & 20)
 Sheet 2 created to move notes off main schematic
- Ver 0.3 : PCB Size to be changed to full width of the available space in case
 Restored HD15 VGA connector as will now mount on PCB
 External power connection for FPGA will now mate with PCB
 Added external power source barrel jack connector to PCB
 Deleted PCB mounting holes – not needed for internal only PCB
 Added dual SD & uSD Card Modules
- Ver 0.4 : Modified to use SD Card modules with on board passives (R & Cs)
- Ver 0.4 : Layout and dimension changes



Pin assignment changes during routing

P	Signal	Blocking	PCB
1	/MI33	Pin 2	Pin 23
1	/LEV	Pin 4	Pin 21
1	A003	Pin 6	Pin 5
1	A013	Pin 8	Pin 7
1	A023	Pin 10	Pin 9
1	A033	Pin 12	Pin 11
1	A043	Pin 14	Pin 13
1	A053	Pin 16	Pin 15
1	A063	Pin 18	Pin 17
1	A073	Pin 20	Pin 19
1	RD0	Pin 1	Pin 2
1	RD1	Pin 3	Pin 4
1	RD2	Pin 5	Pin 6
1	RD3	Pin 7	Pin 8
1	GN0	Pin 9	Pin 10
1	GN1	Pin 11	Pin 12
1	GN2	Pin 13	Pin 14
1	GN3	Pin 15	Pin 16
1	BLO	Pin 17	Pin 18
1	BL1	Pin 19	Pin 20
1	BL2	Pin 21	Pin 22
1	BL3	Pin 23	Pin 24

PCB Edge connector optimised for EDAC 345-060-560-201 connectors with 0.64mm x 9.91 mm tails

Sheet: /MFX_notes/
 File: MFX_notes.sch

Title:

Size: A4

Date:

Rev:

KiCad E.D.A. kicad 4.0.7

Id: 2/2