



Version 3 tested & working, version 4 replaces the HCT20 with HCT30 to eliminate one of the HCT138's and Rom7 select now OR'd with *re/cpm as per Mark's suggestions
 Version 5 includes the remainder of Paul's suggestions and *grom replacing rom 7 identification

ROM does 2 jobs

Paged in as ROM 7 it's the controlling software
 Paged in bank 1 of the half ram page, it's the game data store

Paging for rom 7 - R15=0 R14=0 R13=1 R0=1 R1=1 R2=1, X0-X4 =0 *RE/CPM=0
 Paging for Bank1 R15=0 R14=1 P2=0 P3=0 P0/P1=0,1 or 3 for MTX500/MTX512/RS128
 Output port selected when IOWR low(via OR) and A0-A7 all high(via nand)

HC138 inputs 2 low one high CS, and 3 selectors
 for in situ write to flash, the spare gate in hc32 should be wired
 A and B inputs to *WR and *MREQ, Y output then replace 5v to pin 31