MICROPROCESSOR SYSTEMS SERVICING

SERVICING THE BBC MICRO

HARDWARE AND SIMPLE TEST PROGRAMS

MEDC
MICROELECTRONICS EDUCATIONAL DEVELOPMENT CENTRE

INTRODUCTION

The BBC microcomputer comprises a large single PCB, a keyboard PCB and a modular power supply. The circuit is complex and not easy to service, especially as many of the chips are soldered in. An additional, and often serious problem is that many - indeed the great majority - of faults within the main PCB will result in system failure - that is no output from or input to the micro, and no possibility of loading or running test software by conventional means. Servicing a device of this complexity is often a 'seat of the pants' affair, requiring experience and an in-depth knowledge of the hardware. It is the aim of this course to reduce the 'seat of the pants' aspect as much as possible by introducing some standard techniques such as logic and signature analysis, and to increase the delegate's knowledge of machine hardware and assembly language subroutines.

PRELIMINARY CHECKS

If the machine is completely dead check the fuse in the mains plug. Some earlier machines also had a fuse beside the mains switch at the rear.

If peripheral devices are working incorrectly check the points where these plug into the micro. Sometimes the plugs do not click in fully, resulting in bad contacts. Check the leads between the micro and the devices. If possible, check the micro with other similar devices or the devices with another micro. Keep the connections to cassette recorder or disc drives well away from the mains leads or the lead to the TV or monitor.

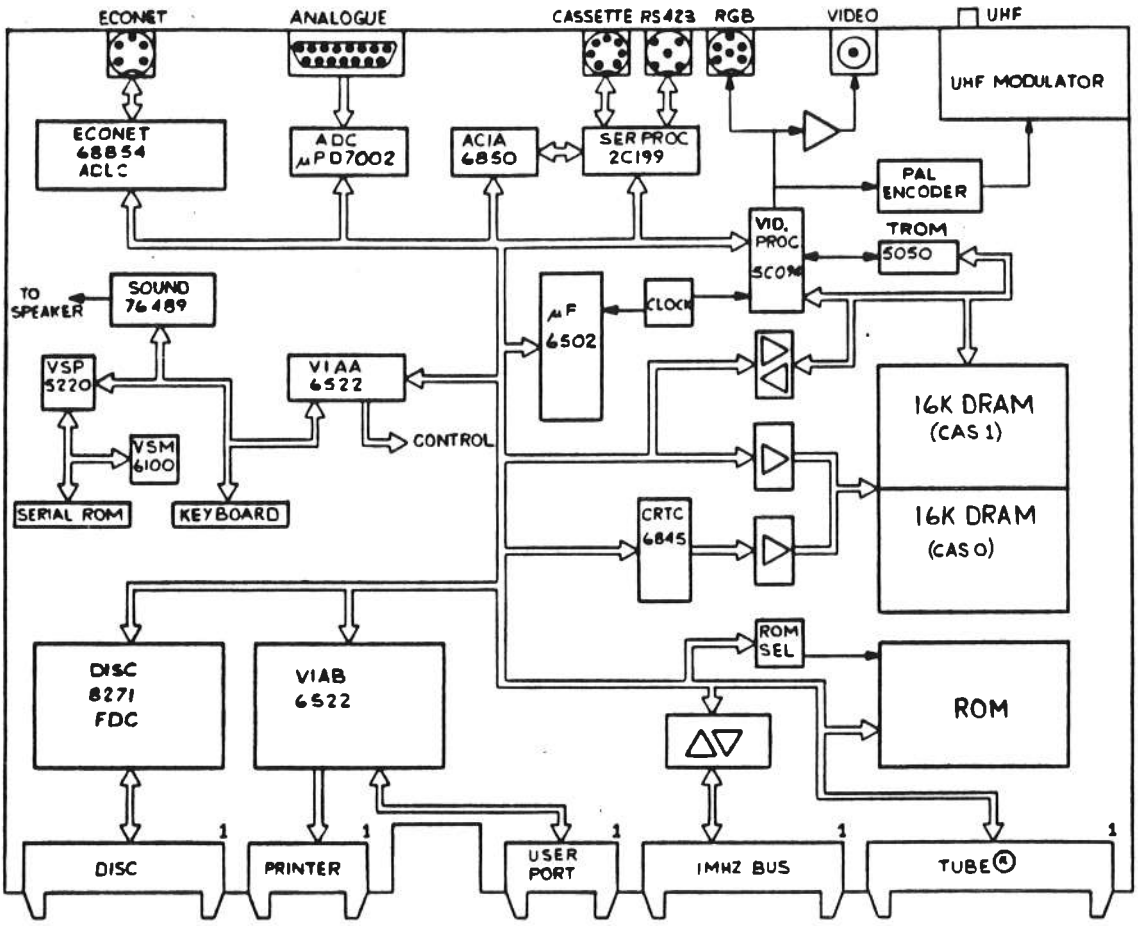
Open the machine by removing the four screws marked 'FIX' - two on the back panel and two on the base. Store these in a safe place. Remove the bolts restraining the keyboard and slide it forward to give access to the full main PCB. Check for signs of damage to the PCB or to components. Choose a stable workspace where the risk of things falling into the machine is at a minimum. Check that the socketed I.C.s are firmly in their sockets. If you know that any of these have recently been replaced or removed and re-inserted, remove the suspect chip and check for bent or broken pins. Re-insert carefully.

Connect the micro to a TV or VDU. Plug in and switch on. Check for any component overheating or smoking. Check that the reported fault is still present.

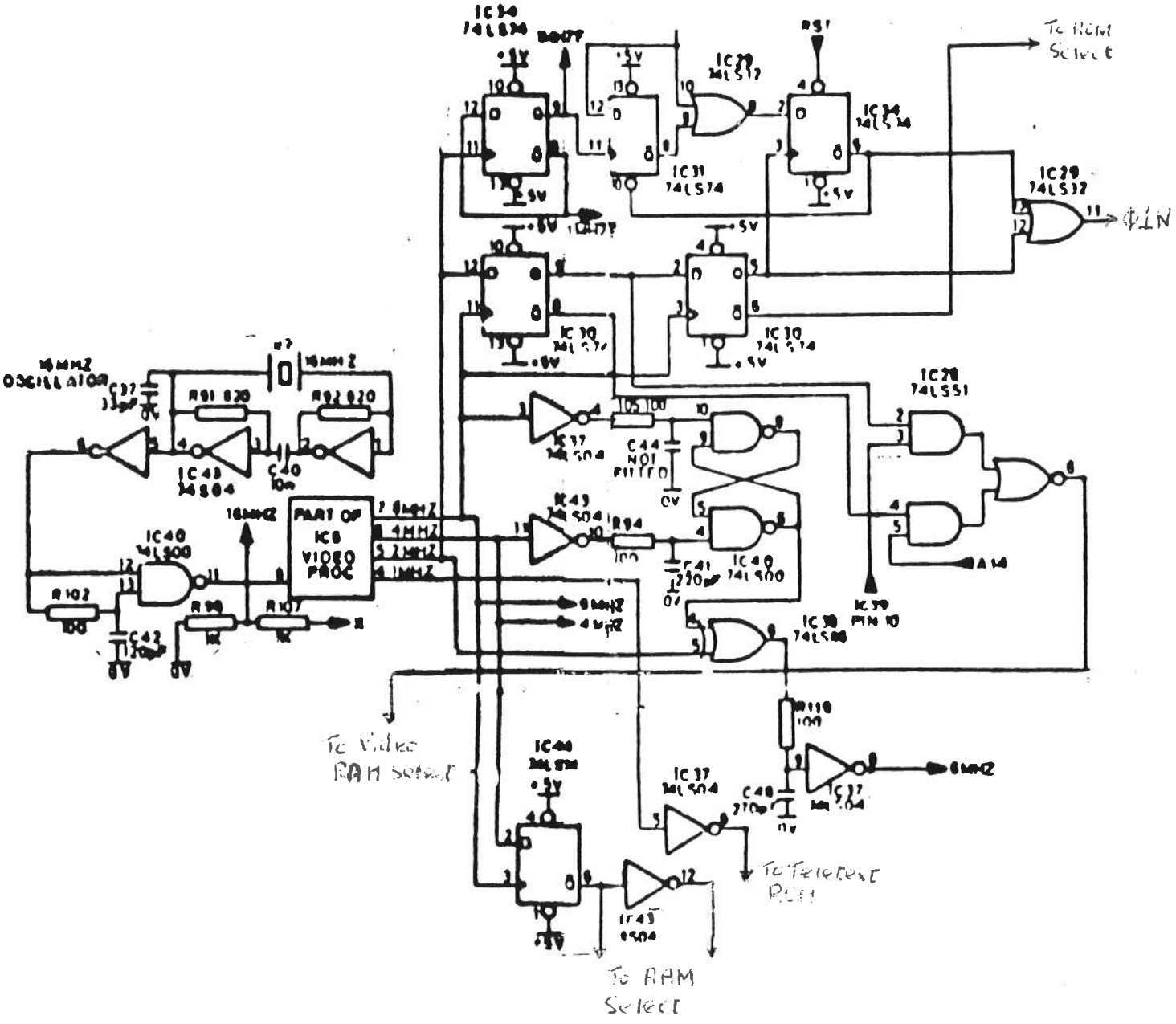
POWER SUPPLY

Check +5v on spade connections Vcc1, Vcc2 and Vcc3. Check +5v on keyboard - 3rd connector pin from your right as you face the machine. Check also the positive lead of the 22 microfarad keyboard decoupling capacitor.

Check the -5v connector. Note that if the -5v supply is not present the machine will still run, but certain peripherals (eg. cassette recorder) will not work properly.



Block Diagram



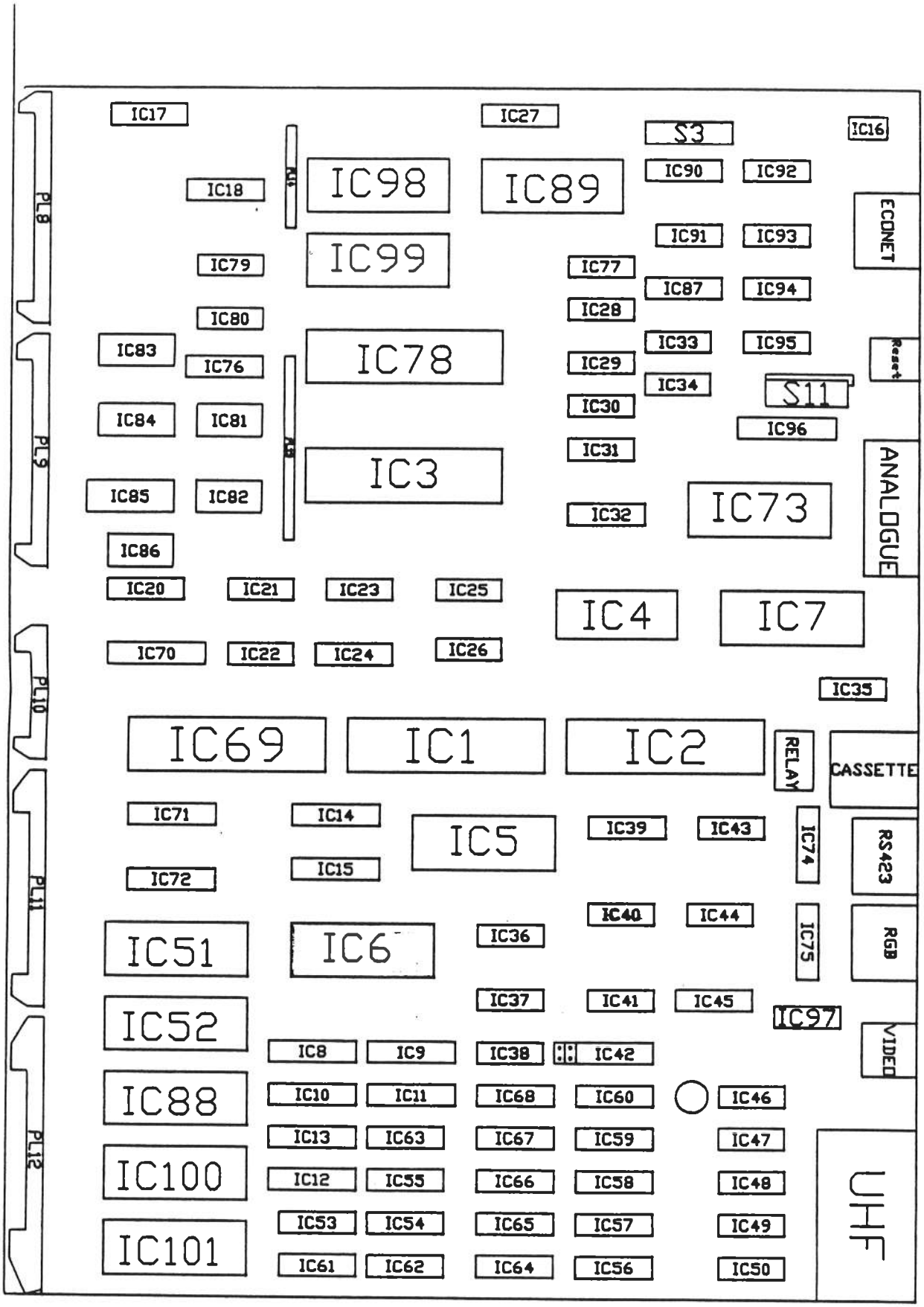
Clock Generation and distribution

The power supply is a modular unit and should be replaced if faulty. Attempted repair is not advised.

CLOCK CIRCUITRY

A 16 MHz crystal controlled oscillator uses three buffers in IC 43. The signal is fed via a spike filter implemented using one gate of IC 40 into the video processor ULA,IC6. Pins 4, 5, 6, and 7 IC6 produce 1, 2, 4 and 8 MHz clocks in phase. A D-type flip flop (half of IC 34) divides the 2 MHz signal in order to produce the system 1 MHz clock. A 2 MHz signal of suitable phase is produced at the output of another D-type (half of IC 30) and this is further clocked through the second D-type (half of IC 30), and through an OR gate producing the normal 2 MHz clock input to the microprocessor. Requests for a 1 MHz processor cycle from the address decoding are fed via an inverter (1/16th of IC 33) to the D-type (half of IC 31) which remembers that a 1 MHz cycle has been requested. At the appropriate time, as governed by the 2 MHz clock, one of the 2MHz clock cycles is masked off by the D-type (half of IC 34) and when this happens the D-type that remembered that a request had been made is cleared.

A 6 MHz clock signal is required for the Teletext character generator (IC 5). This signal is produced by knocking a reset flip flop (two quarters of IC 40) backwards and forwards from 8 MHz and 4 MHz clock signals. The resulting flip flop output is then itself inverted according to the state of the 2 MHz clock signal by an exclusive OR gate (one quarter of IC 38). Glitches on this output are removed by R1129 and C48 to produce the 6 MHz clock signal at Pin 8 of IC 37.



BBC Printed Circuit Board

Chips involved in clock circuitry

EXERCISE

Ensure that the machine is in Mode 7 by pressing the BREAK key.

Using an oscilloscope and frequency meter, record the waveform and frequency of the signals on the pins listed below. Note that the 16 MHz clock may not register on the frequency meter. (IC 43 pin 6 and IC 40 pin 11).

IC 43	pin 6	.....
IC 40	pin 11	.....
IC 6	pin 8	.....
	pin 7	.....
	pin 6	.....
	pin 5	.....
	pin 4	.....
IC 44	pin 6	.....
IC 43	pin 12	.....
IC 37	pin 8	.....
IC 34	pin 8	.....
IC 34	pin 9	.....
IC 30	pin 8	.....
IC 30	pin 9	.....
IC 40	pin 6	.....
IC 30	pin 5	.....
IC 30	pin 6	.....
IC 1	pin 37	.....
IC 1	pin 39	.....
IC 1	pin 3	.....

Keyboard connector
-3rd from your left when
facing machine ....

Enter and RUN the following program:

```
10   P% = &4000
20   [       SEI
30   .START  STA    &FE00
40           STA    &FE00
50           JMP    START
60   ]
```

Start the machine code program with CALL &4000.

The clock to the CPU (IC 1 pin 3) should alternate in frequency between 1MHz and 2MHz. The frequency meter should average this reading at 1.5 MHz. Note the fairly distinctive pattern this produces on the oscilloscope.

Note the pattern and frequency of the signal on the Read/Write line while the machine code program is running:

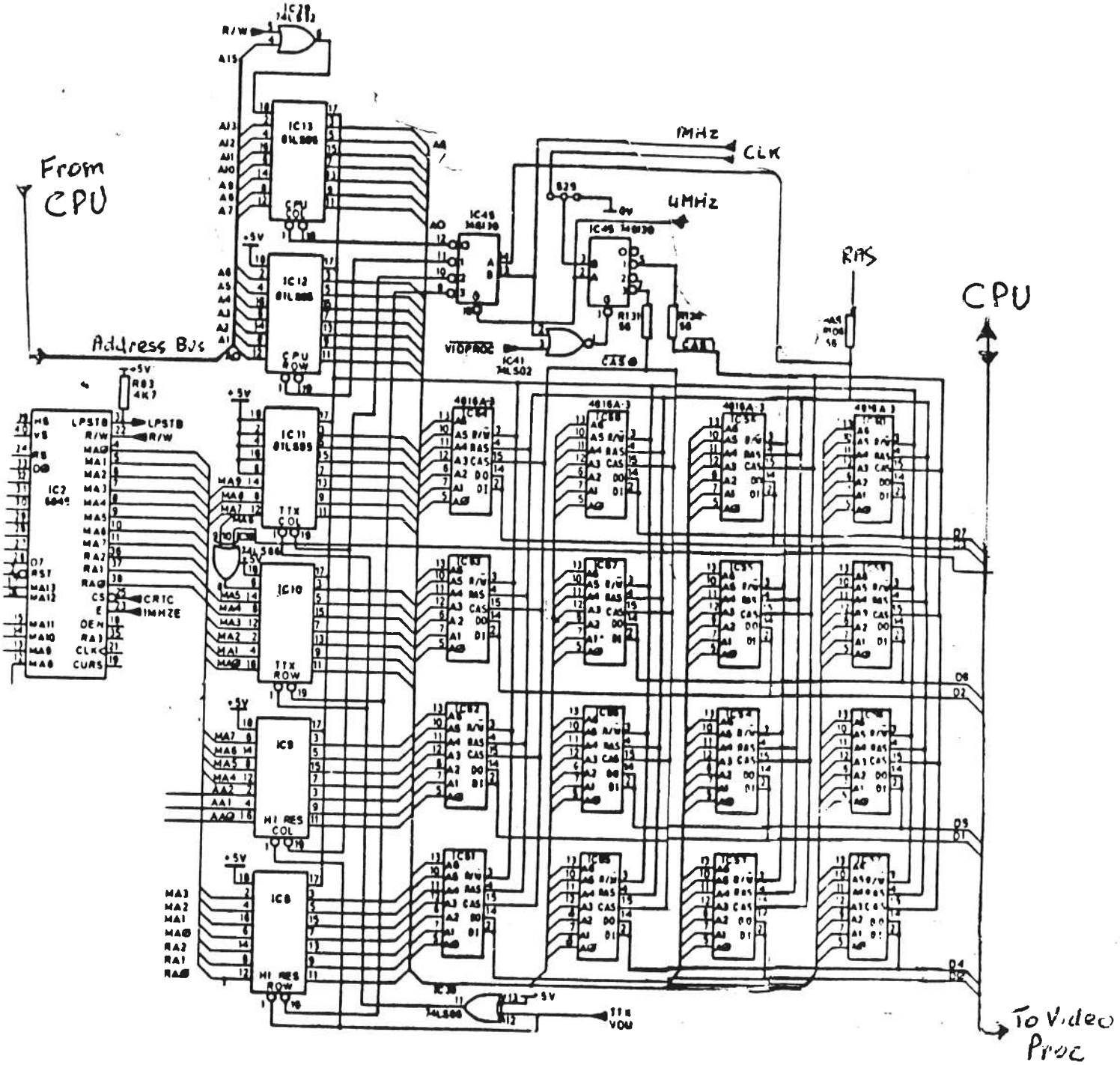
IC 1	pin 34	.....
IC 33	pin 12	.....
IC 33	pin 10	.....

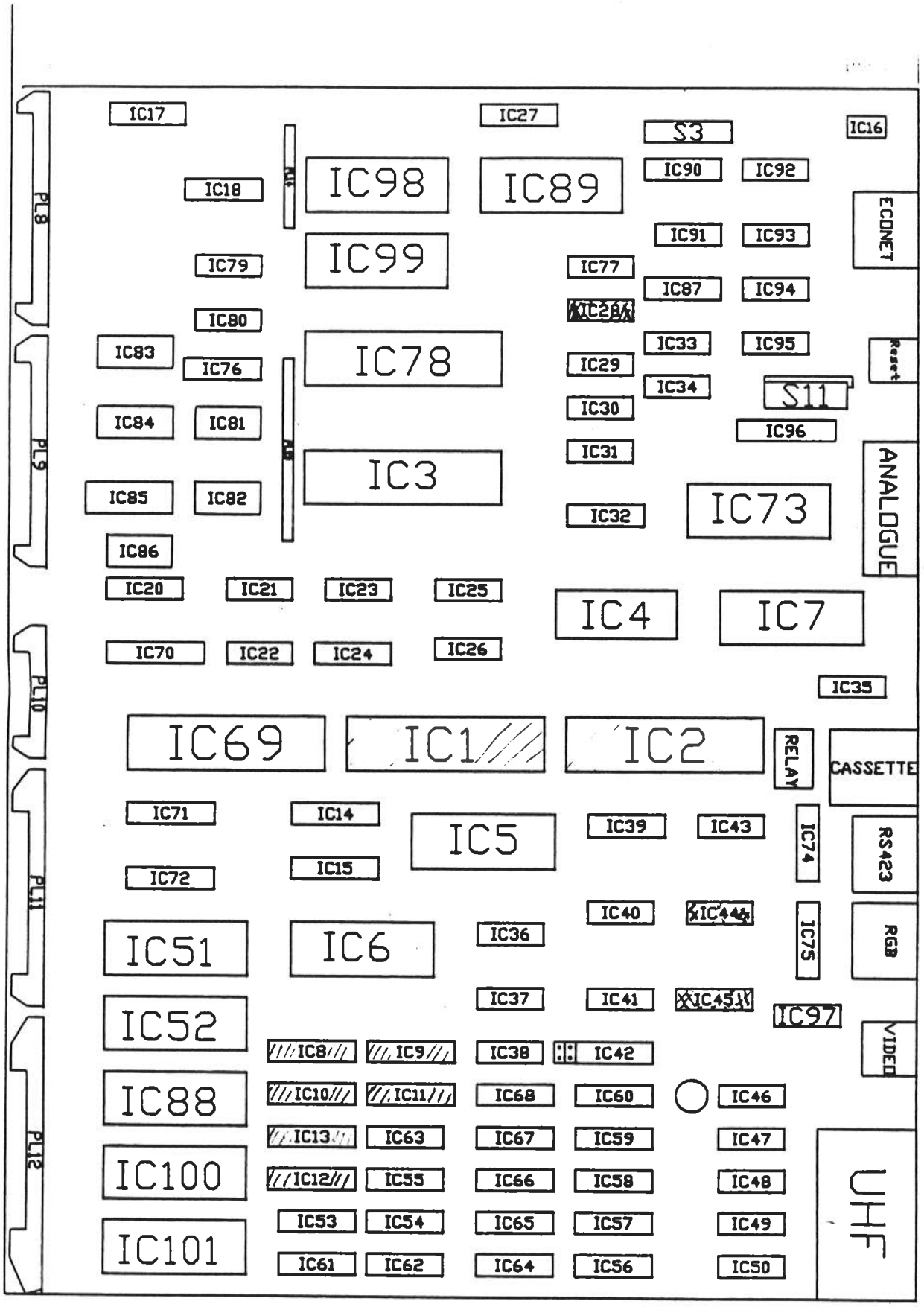
Stop the program by pressing BREAK.

RANDOM ACCESS MEMORY

Random Access Memory on the Microcomputer is provided by either 8 or 16 dynamic memory devices (ICs 53-68). The row address strobe and column address strobe signals for these RAMs are cycled constantly at 4 MHz. Two devices may have control of the RAM address lines, one is the 6502 Microrocessor and the other is the 6845 cathode ray tube controller chip (IC 2). The Cathode Ray Integrated Circuit generates the raster scan signals for the video display, together with the address for each memory mapped byte of information in the RAMs which is required to refresh the display. Six octal buffers, type 81LS95 (ICs 8-13) are used to switch control of the RAM address lines between the Microprocessor and the CRIC.

Every 250 nanoseconds control of the RAM address lines is switched between the Microprocessor and the CRIC. Thus, in a one microsecond period, the Microprocessor has two RAM accesses and the CRIC has two RAM accesses. Because the CRIC generates a sequence of addresses in order to refresh the display, the row


From CPU
Address Bus
R/W
A15
IC13
IC12
IC11
IC10
IC9
IC8
IC2
6845
IC41
74LS02
IC38
74LS86
IC45
74LS30
IC46
74LS30
1MHz
CLK
4MHz
0V
RAS
CPU
CAS
VIDPROC
+5V
R83
4K7
LPSTB
R/W
CRTC
1MHZE
CURS
TTX COL
TTX ROW
HI RES COL
HI RES ROW
TTX VDU
To Video Proc
RAM



BBC Printed Circuit Board

RAM and RAM control

address lines of the RAMs are also refreshed by virtue of the sequential CRIC accesses.

The dynamic RAMs are constantly cycled by a row address strobe (RAS) signal which is produced by a D-type connected to the 8 and 4 MHz clock signals (half of IC 44). This RAS signal then drives all of the dynamic RAMs via R106. The dynamic RAMs are divided into two banks of 16 kilobytes, that is two banks of 8 RAMs. These banks are input or output enabled by virtue of having their column address strobe (CAS) available. In Model A computers with only one bank of RAM only CAS 1 is used. 32 Kilobyte computers have a second bank of RAMs selected by a 74LS51 circuit (IC 28) which controls the 74S139 (half of IC 45) producing the CAS signals. The other half of 74S139 (half of IC 45) is used to select between the processor and CRIC address lines.

EXERCISE

Using the oscilloscope and frequency meter, record the waveform and frequency of the signals on the following pins:

IC 2	pin 23	.....
IC 2	pin 36	.....
IC 2	pin 37	.....

Ensure that the machine is in Mode 7 by pressing the BREAK key.

Enter and RUN the following program (Model B only).

```
10   P% = &3000
20   [      SEI
30   .START    LDA &5000
40             JMP START
50   ]
```

Start the machine code program with CALL &3000

Note the waveform and frequency of the signals on the following pins:

IC 45	pin 3	.....
IC 64	pin 15	.....
IC 45	pin 5	.....
IC 53	pin 15	.....

Break from the program. Enter OLD then LIST
Change the program to:

```
10   P% = &3000
10   [         SEI
30   .START    LDA &3000
40             JMP START
50   ]
```

RUN this program and start the machine code routine with CALL &3000.

Note the waveform and frequency of the signals on the same pins as before - i.e.

IC 45	pin 3	.....
IC 64	pin 15	.....
IC 45	pin 5	.....
IC 53	pin 15	.....

Break, enter 'OLD' and LIST the program as before.
Change to:

```
10  P% = &5000
20  [           SEI
30  .START      LDA &5000
40              JMP START
50  ]
```

RUN the program and CALL &5000.

Note the frequency and waveform of the signals on:

IC 45	pin 5	.....
IC 53	pin 15	.....

Note there are no pulses on IC 45 pin 3 and IC 64 pin 15. Explain this.

VIDEO DISPLAY

Because of the way the CRIC accesses RAM, two bytes of information are available per microsecond for refreshing the raster scanned video display. With each horizontal line having a period of 64 microseconds, a 40 microseconds active display area is usual. Thus, 640 bits of information per horizontal line are produced from the memory mapped display.

The video processor device (IC 6) is a custom made uncommitted logic array developed especially for use in this Microcomputer. At the end of each CRIC 250 nanosecond access period, it latches the byte from the RAM and, according to the display mode in operation, serialises the byte into one bit stream of 8 bits or two bit streams of 4 bits etc. In this way, display modes varying from 640 pixels in 2 colours to 160 pixels in 8 colours, which may or may not be flashing, can be produced.

Also in the video processor is a high speed section of static Random Access Memory called a palette. This memory can be programmed to define the relationship between the logical colour produced by the RAM and the physical colour which will appear on the display. Thus, in a 640 pixel mode, the two colours to appear on the display need not be black and white, they may be, say, red and blue. Note that the information in the RAM is unchanged by the palette; it is its interpretation into physical colours which changes.

Modes 0 through 6 in the Microcomputer use software generated characters, that is to say, the character font to be produced on the screen is held in the memory mapped display area of the RAM and graphics or characters may be held. This method of producing characters is expensive in memory, involving a minimum of 8 kilo-bytes for the display memory.

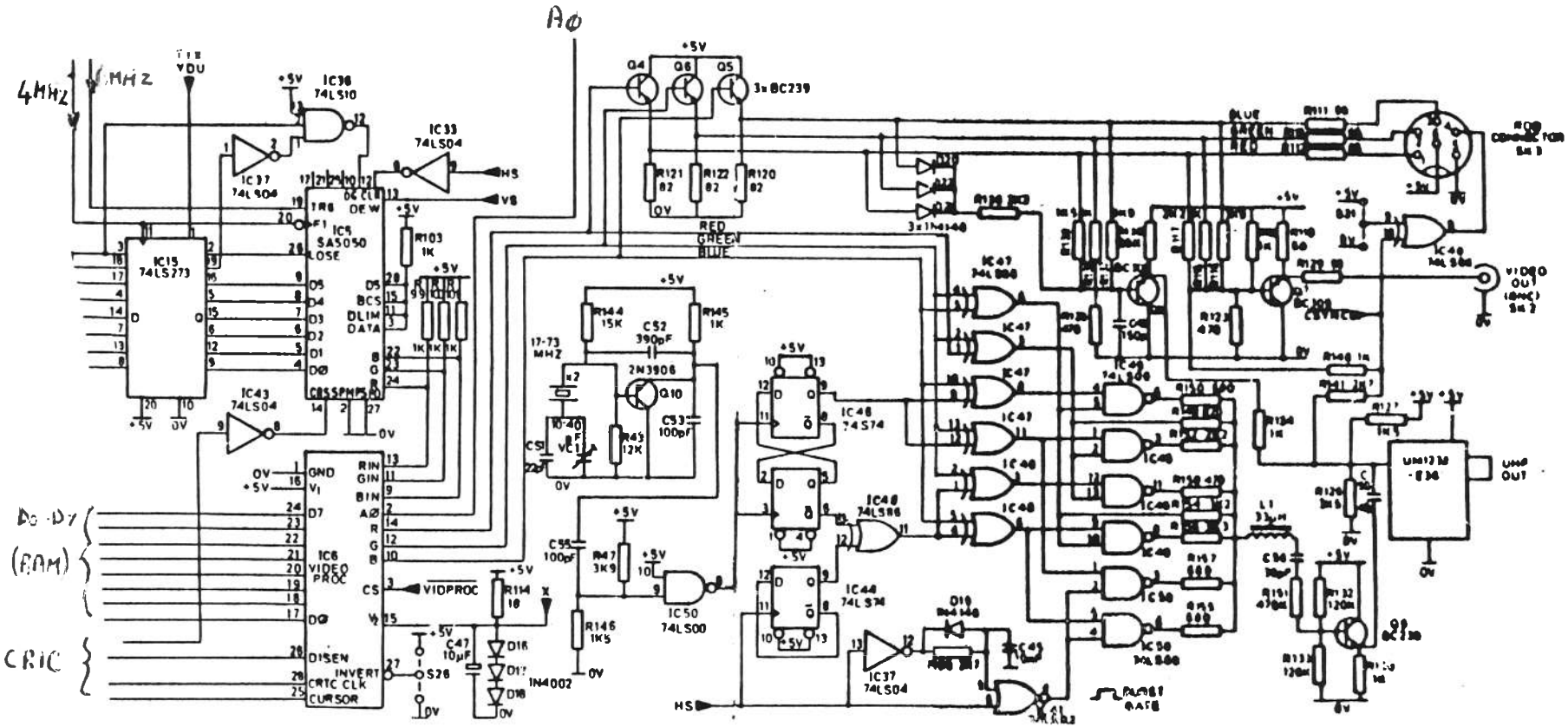
Display mode 7 is a Teletext mode and to implement this an SAA 5050 (IC 5) Teletext character generator Read Only Memory is used. IC 15 latches the information coming from the RAM prior to SAA 5050. When using this mode, only 1K of RAM is devoted to the display memory and the characters are held within it as ASCII bytes. The SAA 5050 then translates these bytes into a standard Teletext/Prestel format display.

The red, green and blue logic signals produced by the video processor are buffered by transistors Q4, 5 and 6 and fed out together with a composite sync signal to the RGB connector (SK3). This output is suitable for feeding straight to the gun drives of RGB monitors. The red, green and blue lines are summed together by binary weighted resistors to feed Q7 which produces a 1v composite video signal suitable for feeding to monochrome monitors, on which the different colours will appear as different shades of grey.

Also available from the main printed circuit board is a UHF TV signal on channel 36, suitable for feeding to the aerial input of a domestic television. This output is modulated by an Astec modulator. Colour is provided for domestic televisions by a PAL

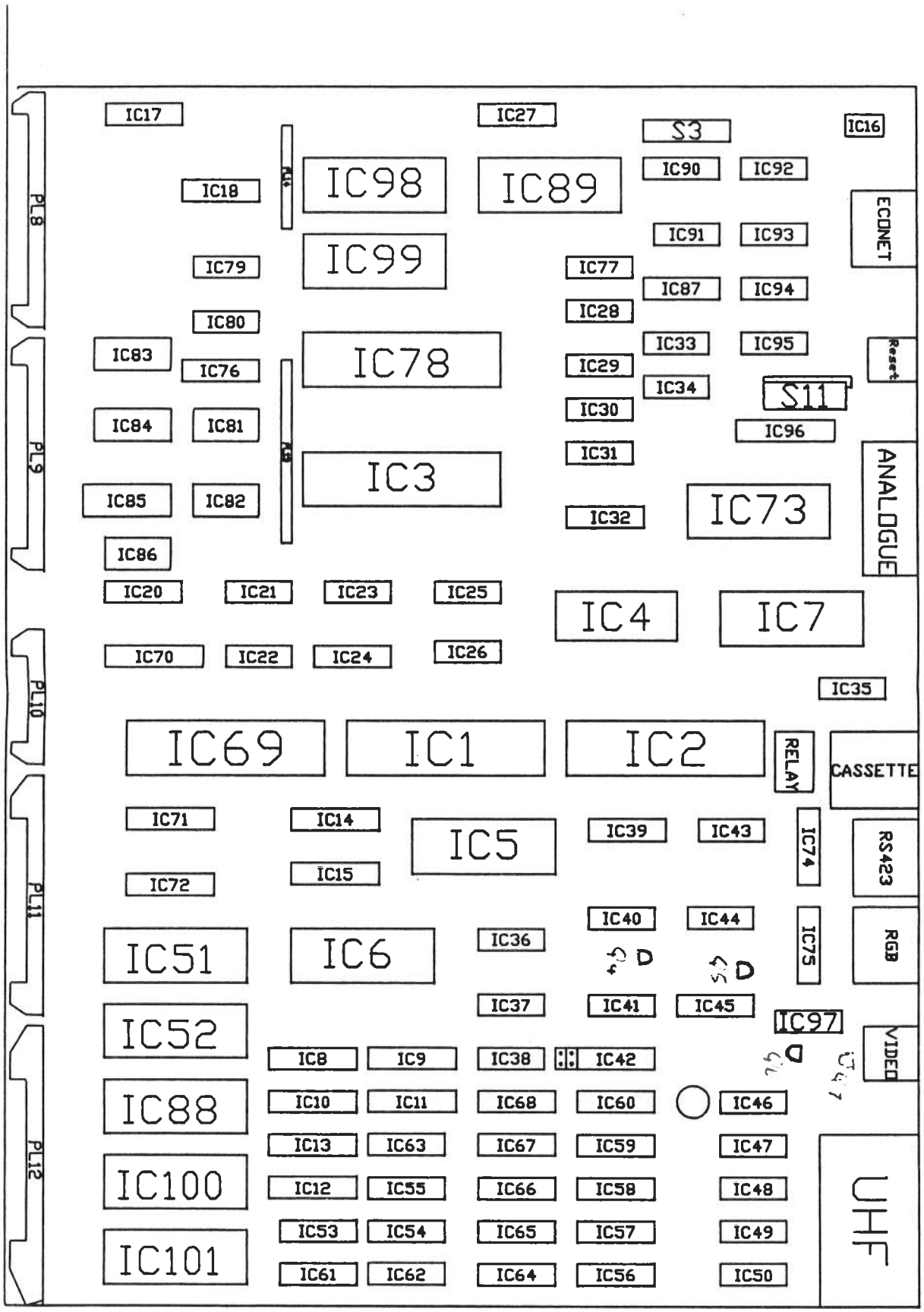
(phase alternating line) encoder circuit which modulates the colour information on to the colour subcarrier frequency. Q10 is a 17.73 MHz oscillator circuit which is divided by a ring counter (IC 46) giving 2 outputs at the colour subcarrier frequency of 4.43361875 MHz. One of these two outputs is switched by the horizontal line frequency in order to produce the alternate phase on each TV line. Thus, on IC 46, pin 9, we have the 'U' and 'V' signals according to whether a red, green, blue, cyan, magenta, yellow or white colour is to be produced. These signals then drive resistors via a row of AND gates in order to produce the colour subcarrier signal which is added to the monochrome output from Q8 by the buffer Q9.

In order that the receiving television can interpret the colour information, a reference colour burst has to be provided at the beginning of each line. A short burst gate signal immediately after the horizontal sync pulse for each line is produced at Pin 4 of IC 41, and it is timed by C45 and R109. This burst gate allows through a standard colour subcarrier signal which the television uses as its reference for the rest of that line. The PAL signal may be added to the 1v video connector with the addition of a 470 pF capacitor between the emitter of Q9 and the base of Q7. Diodes D20, 21 and 22 increase the luminance of the darker colours, e.g. blue, in order to make coloured text displays more readable.



Video Display

BBC Printed Circuit Board



Components in video display circuitry

EXERCISE

Ensure that the machine is in Mode 7.

Note the frequency and waveform of the signals on the following pins:

IC 5	pin 10	.....
IC 5	pin 12	.....
IC 5	pin 1	.....
IC 5	pin 20	.....

Put the machine into Mode 2 (Model B only)

Note the new waveform and frequency on:

IC 5	pin 14	.....

In Mode 2, enter and RUN the following program:

```
10  REPEAT
20  FOR N = 128 TO 135
30  COLOUR N
40  CLS
50  A$ = INKEY$(50)
60  NEXT
70  UNTIL FALSE
```

Use an oscilloscope to look at the signals on the following pins:

IC 6	pin 10	.....
IC 6	pin 12	.....
IC 6	pin 14	.....

Trace these signals through the emitters of Q5, Q6 and Q4 respectively to pins 3, 2 and 1 of the RGB socket.

Note the composite signal on the emitter of Q7. Explain the d.c. voltage 'steps' of the peak positive value of this circuit.

Note the signals on:

IC 47 pin 3 .....

IC 47 pin 6 .....

IC 47 pin 8 .....

IC 47 pin 11 .....

IC 48 pin 3 .....

IC 48 pin 6 .....

IC 49 pin 3 .....

IC 49 pin 6 .....

IC 49 pin 8 .....

IC 50 pin 3 .....

IC 50 pin 6 .....

Relate the changes of signal at these pins to the colours on the screen.

Note the signal and frequency of the burst gate signal on:

IC 41 pin 4 .....

Note waveform and frequency on :
~~the d.c. level change on:~~

IC 47 pin 9 .....

Note the waveform and frequency on:

IC 48 pin 11 .....

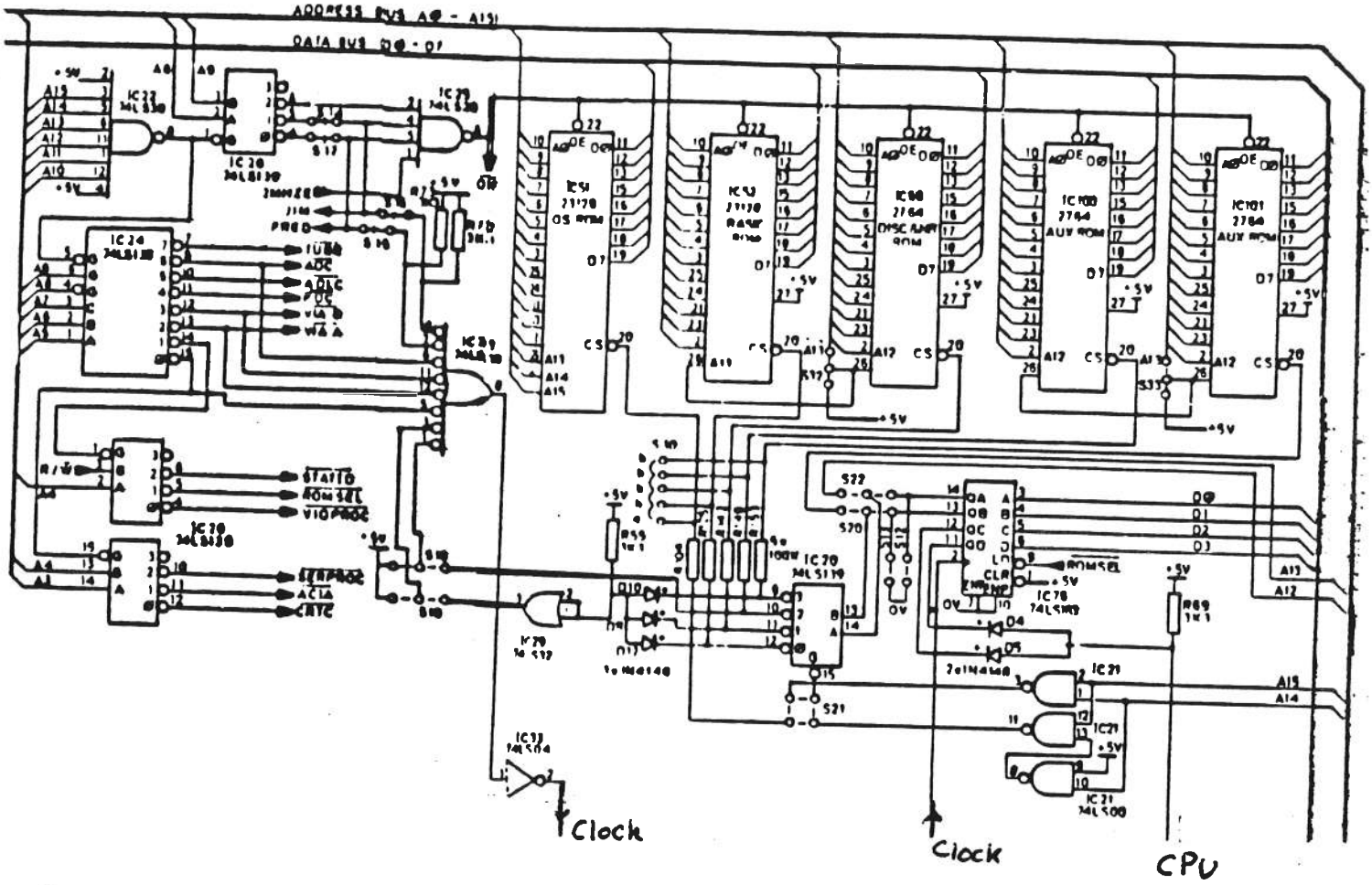
Escape from the program and put the computer in Mode 7.

READ ONLY MEMORY

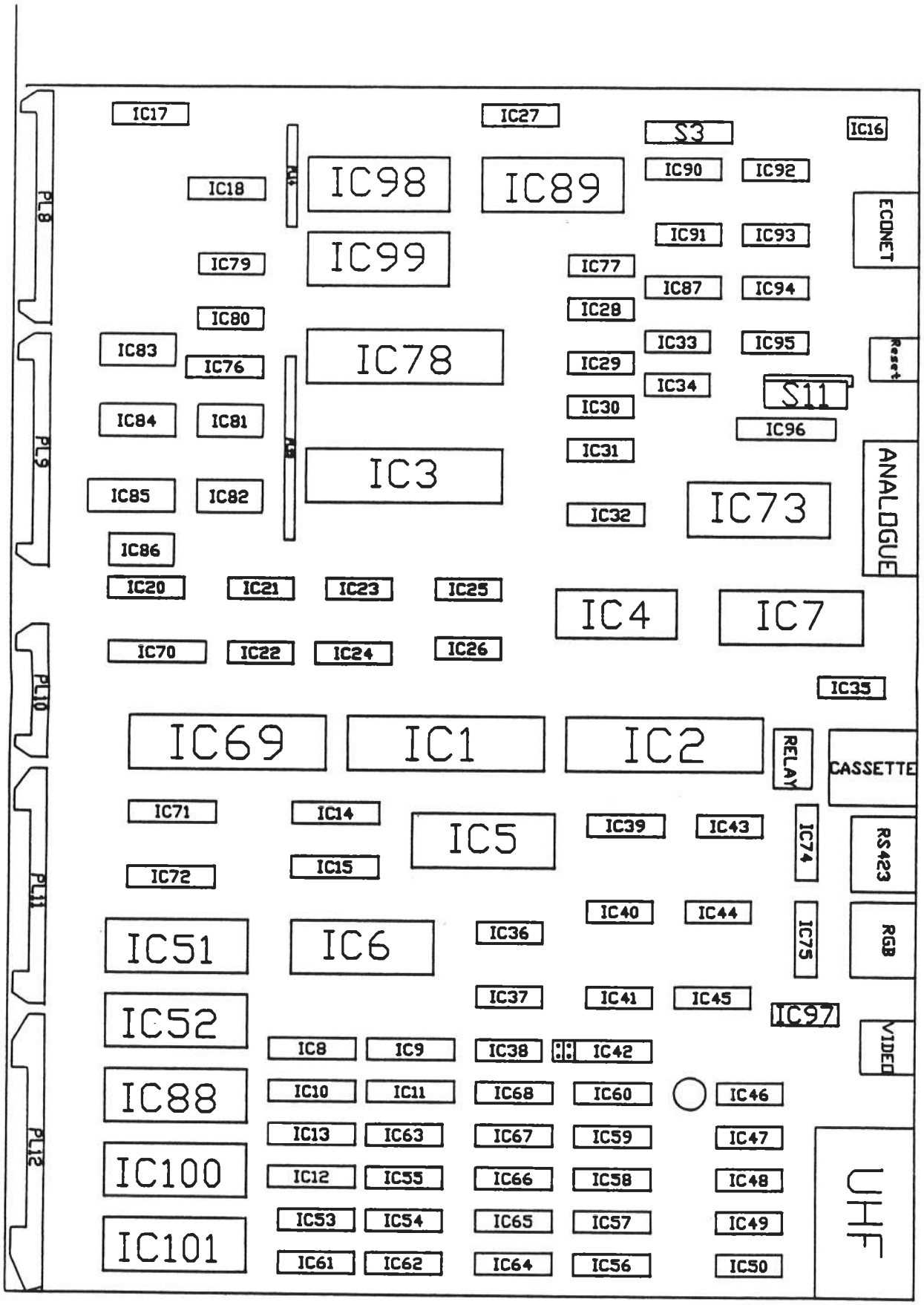
31 kilobytes of Read Only Memory are catered for in the Microcomputer address map. 15 kilobytes of this is contained in the operating system Read Only Memory (IC 51). This is, in fact, a 16K device but 1K of it is left unused and it is in this area that the hardware memory map is situated. Four other Read Only Memories (ICs 52, 88, 100 and 101) are on the main circuit board. Cosiderable flexibility is offered by these ROMs. They may all be 16 kilobyte devices, in which case any one of them may be switched into the 16 kilobyte space in the memory map by writing to the ROM select latch (IC 76). Alternatively, four 4 kilobyte ROMs may be in these four sockets in order to fill the 16 kilobyte spaces assigned. In this case, a two line to four line decoder (half of IC 20) is used to select which of the four devices is being addressed by the address lines A12 and A13.

Mixtures of these two cases are allowed for, for instance two pairs of 8 kilobyte ROMs, one pair or the other being selected by the ROM select latch and then the ROM to be used in each pair being selected by the 2-4 line address decoder. Normally, IC 52 will contain the resident BASIC interpreter and ICs 88, 100 and 101 will contain either other languages such as Pascal, or extra system software such as a Disc Filing System.

Address decoding for the ROMs is by IC 21 which decodes memory addresses 8000 to C000 and C000 to FFFF (hex). Locations from 0 - 7FFF (hex) are assigned to the dynamic RAM and this is decoded by feeding A15 into pin 4 of IC 21. All the rest of the hardware is located within locations F000 to FBFF (hex). This is decoded by IC 22 and via ICs 20 and 25, the Read Only Memory is then masked off over this range of addresses. ICs 24 and 26 decode the individual devices in this range, some of which are read or write only. IC 23 detects when a slow 1 MHz device is being addressed and it calls for the 6502 to do a slow clock cycle.



ROM and general decode circuitry



BBC Printed Circuit Board

ROM and ROM control

EXERCISE

Chequerboard test of address lines.

Load and RUN the following program.

```
10   P% = &3000
20   [          SEI
30   .LOOP      LDA &5555
40              LDA &AAAA
50              JMP LOOP
60   ]
```

Start the machine code subroutine with CALL &3000

Determine and note the frequency of the signal on address lines A0 to A15 (IC 1 pins 9 to 20, 22 to 25)

A0	(IC 1 pin 9)
A1-A3	(IC 1 pins 10-12)
A4-A15	(IC 1 pins 13-20, 22-25)

With a dual beam oscilloscope, note the relationship of the signals on adjacent address lines A4 and A5 and on address lines A4 and A6. Explain this.

The signals generated by this test may be traced through the circuit from chip to chip to check for broken tracks, dry joints etc. Shorts between lines or to ground may also be detected, although in practice these faults will probably inhibit test program entry.

The signals generated by this test do not appear on the RAM chip address pins. Why not?

Because of the flexibility of the ROM select circuitry, the next test may have to be adapted for particular configurations. The program as it stands exercises chip selects of ROM at the bottom and at the top of the ROM section of the memory map.

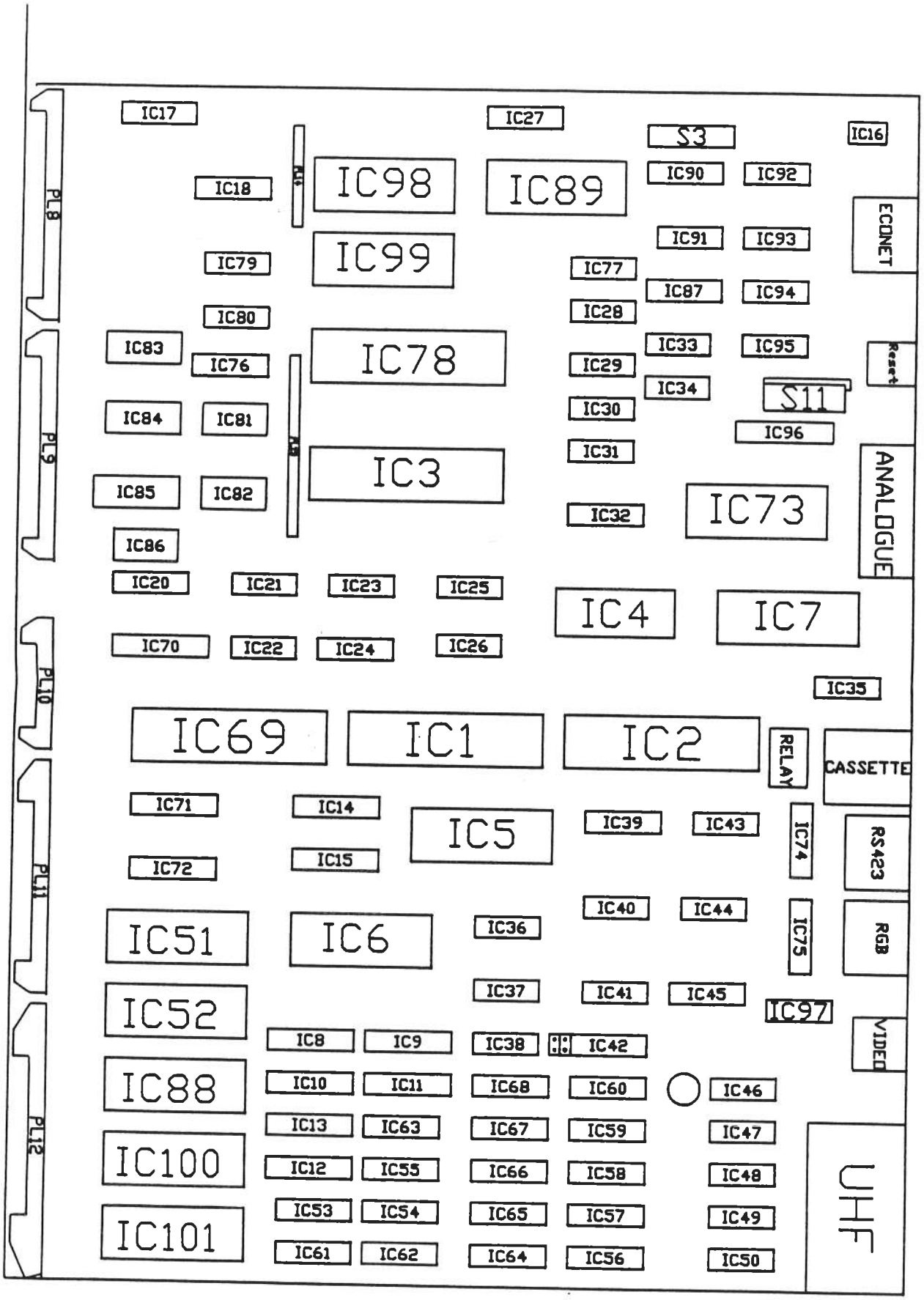
```
10   P% = &3000
20   [          SEI
30   .LOOP      LDA &8001
40              LDA &FD00
50              JMP LOOP
60   ]
```

Run the program and start the machine code with CALL &3000. Note the waveform and frequency of the signals on pin 20 of the ROM chips occupying the relevant address positions.

INTERNAL CONTROL

One 6522 VIA device (IC 3) is devoted to internal system operation. Port B drives an addressable latch which is used to provide read and write strobe signals for the speech interface, the keyboard and the sound generator chip. Also, coming from this latch (IC 32) are control lines C0 and C1 which indicate the amount of RAM devoted to the display memory to be 1K or 16K, 8K, 10K and 20K.

BBC Printed Circuit Board



Internal Control

Pins 6 and 7 of the addressable latch drive the capitals' lock and shift lock LEDs on the keyboard. The rest of Port B on the internal system VIA is used to input the two 'fire button' signals from the analogue to digital convertor interface and two response lines from the speech interface. Each time the system VIA is written to any changes on Port B which should affect the addressable latch are strobed into the latch by a flip flop which is triggered from the 1MHz clock signal. Port A of the system VIA (IC99) is a slow data bus which connects to the keyboard, the speech system chip (if fitted) and the sound generator.

EXERCISE

Enter and RUN the following program:

```
10  REPEAT
20  FOR N=0 TO 7
30  MODE N
40  NEXT
50  UNTIL FALSE
```

Record the waveforms on the following pins using an oscilloscope:

IC 32 pin 9 .....

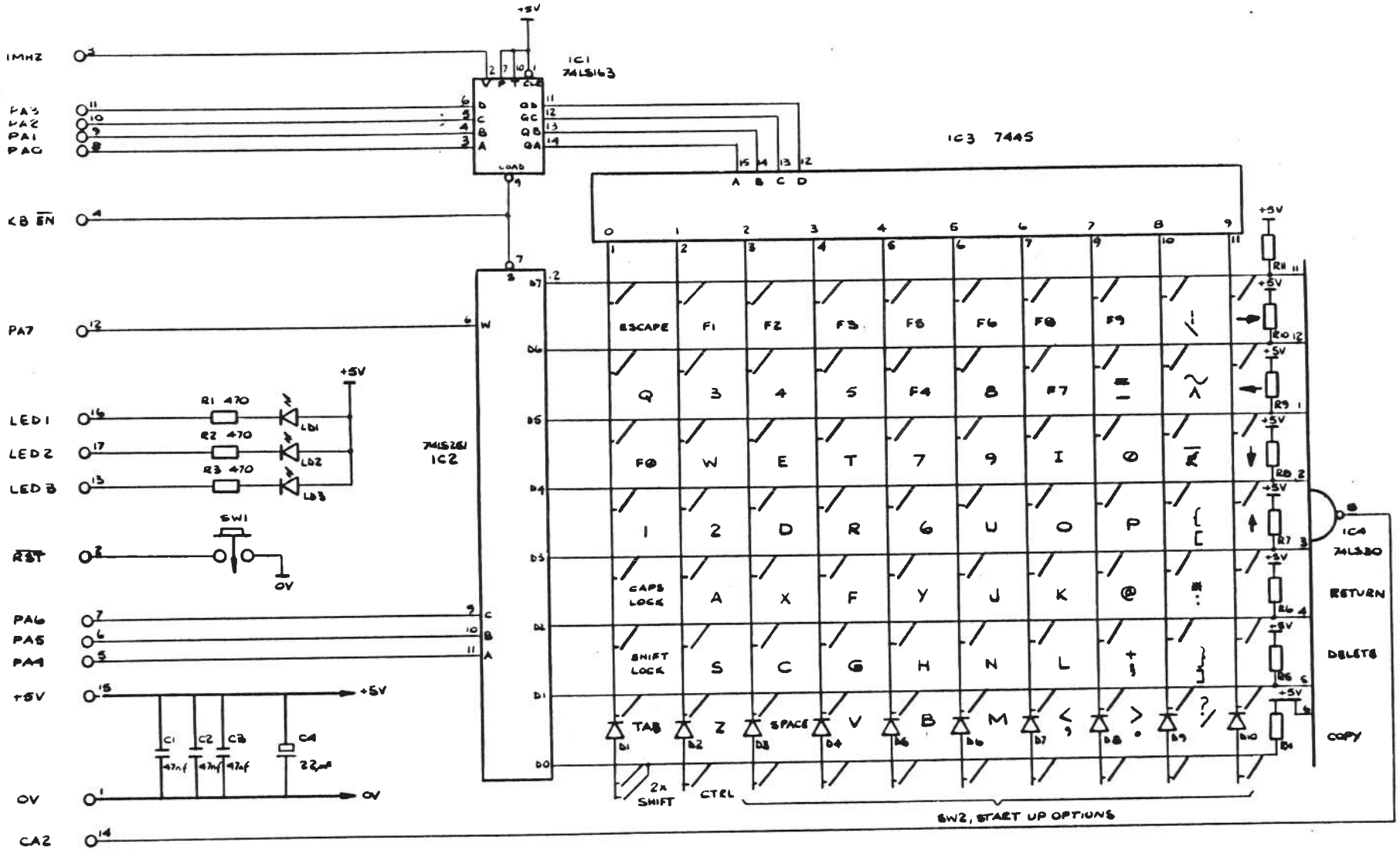
IC 32 pin 10 .....

Note - these waveforms are too low a frequency to give an accurate reading on most frequency meters.

KEYBOARD

The keyboard consists of a ten by eight matrix of normally open contact switches which are mounted on a metal plate. Connections to the contacts of these switches are made by a glass-fibre printed circuit board. This board also carries ICs 1, 2, 3 and 4, the loudspeaker, three LEDs, the keyboard connector (to PL13) and the ROM cartridge socket (if fitted).

The keyboard circuitry is based on the "walking zero's" technique. IC 1 is a synchronous binary counter (74LS163) which is clocked by the 1 MHz system clock. The outputs from this IC are decoded by IC 3 which is a BCD to decimal decoder (7445). The ten outputs of this decoder are connected to the column lines of the keyboard matrix. In this way, each column in turn is pulsed low then high thus producing the "walking zero'" pattern.



NOTE ALL DIODES IN4116

R4-11 10KΩ

Keyboard.

Depression of any key results in the output of IC 4, an 8 input NAND gate (74LS30), pulsing high as the walking zero passes the column to which that key is connected. The output from IC 4 interrupts the microprocessor using the CA 2 line of the system VIA (IC 3). On recognition of this interrupt, the computer executes the keyboard reading routine to discover which key was depressed. This is achieved by latching the BCD address of each column in turn directly into IC 1 using outputs PA0 to PA3 of IC 3, the system VIA, thus interrogating each column in turn. At the same time outputs PA4, 5 and 6 of the system VIA are used to load data into IC 2, which is a data selector (74LS251). Each row is selected in turn by the three bit code present on PA4, 5 and 6. The logic level on a particular row appears at the output of the data selector when selected. In this way, the keyboard matrix is scanned for the coincidence created when a key has been depressed.

EXERCISE

Note the frequency and waveforms on the following pins on keyboard chip IC 1 (74LS163):

pin 2 .....

pin 11 .....

pin 12 .....

pin 13 .....

pin 14 .....

pin 15 .....

With the oscilloscope probe on pin 8 of the keyboard chip IC 4 (SN74LS30) press every key except BREAK, SHIFT and CTRL. A pulse should appear on the trace.

REPEAT this test with the probe on pin 39 of IC 3 on the main PCB.

Note the frequency of the signal on IC 3 pin 6 when a key from each row is pressed in turn (not the BREAK, SHIFT or CTRL keys)

Row 1 (function keys)

Row 1

Row 3

Row 4

Row 5

Repeat the test for IC 3 pins 7 and 8.

RESET

A 555 timer circuit (IC 16) provides a reset signal at power up or when the reset key is pressed. Also on the circuit board is a power up reset CR circuit from the +5 volt power supply (C10 and R20 and D1). This provides a signal called Reset A which is fed to IC 3. Whilst the 555 timer produces a general reset at power up or when the reset key is pressed, the CR signal Reset A only goes low at Power up. By interrogating IC 3 on the occurrences of a general reset, the microprocessor can thus discover whether this is a cold start, i.e. power up, or a warm start, i.e. the reset key being pressed when the system has already been in use.

EXERCISE

Connect oscilloscope to IC 3 pin 34. Switch the machine off and on again. The signal should charge up from 0 to 1. This signal should remain at +5v when the BREAK key is pressed.

Repeat the test with the oscilloscope connected to pin 40 of IC 1 The same effect should be seen on power-up, but this time the signal should go to 0V whenever the BREAK key is pressed.

ANALOGUE TO DIGITAL CONVERTER

A four channel analogue to digital converter facility is provided by IC 73. This device connects straight to the Microcomputer's data bus and it is a dual slope converter with its voltage reference being provided by the three diodes, D6, D7 and D8.

EXERCISE

Check the potential difference between pin 6 of IC 73 and ground, this should be approximately 1.8v.

FLOPPY DISC CONTROLLER

IC 78 is a floppy disc drive controller circuit which is used to interface with one or two, single or double sided, 5 1/4 or 8 inch floppy disc drives. Logic signals from the controller to the disc drive are buffered by two open collector driver packages - IC 79 and 80. The incoming signal from the disc drive is first conditioned by monostable IC 97 producing a pulse train with each pulse of fixed width. These pulses are then fed to the data separation circuits ICs 81 and 82. This is a digital monostable. IC 86 divides the 8 MHz clock signal down to 31.25 K. ICs 83, 84 and 85 are then used to detect index pulses coming in from the drive which show that the drive is ready for a read or write operation.

EXERCISE

Check the frequency of the signals on:

IC 86 pin 1 .....

pin 3 .....

pin 4 .....

pin 5 .....

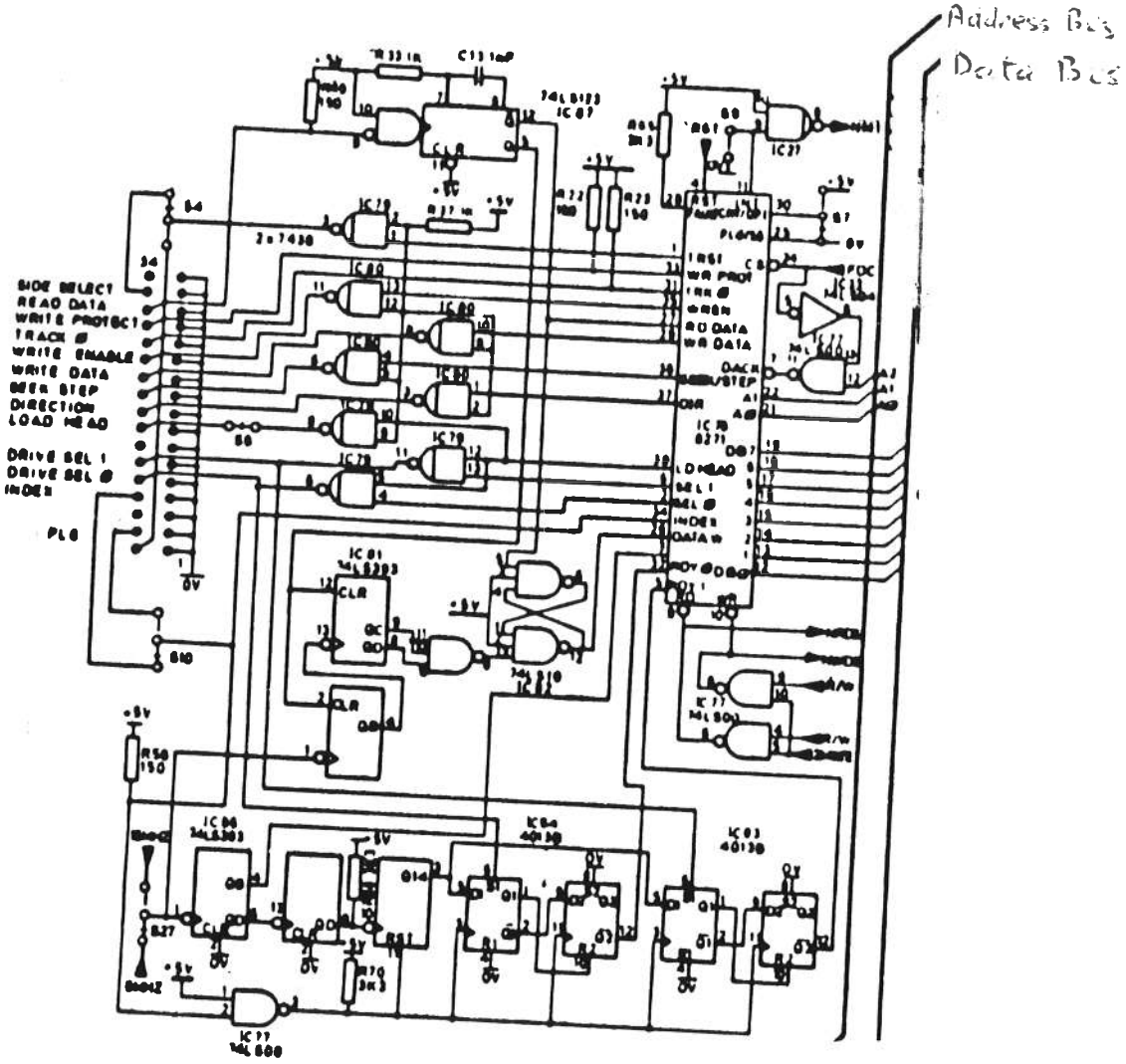
pin 6 .....

pin 8 .....

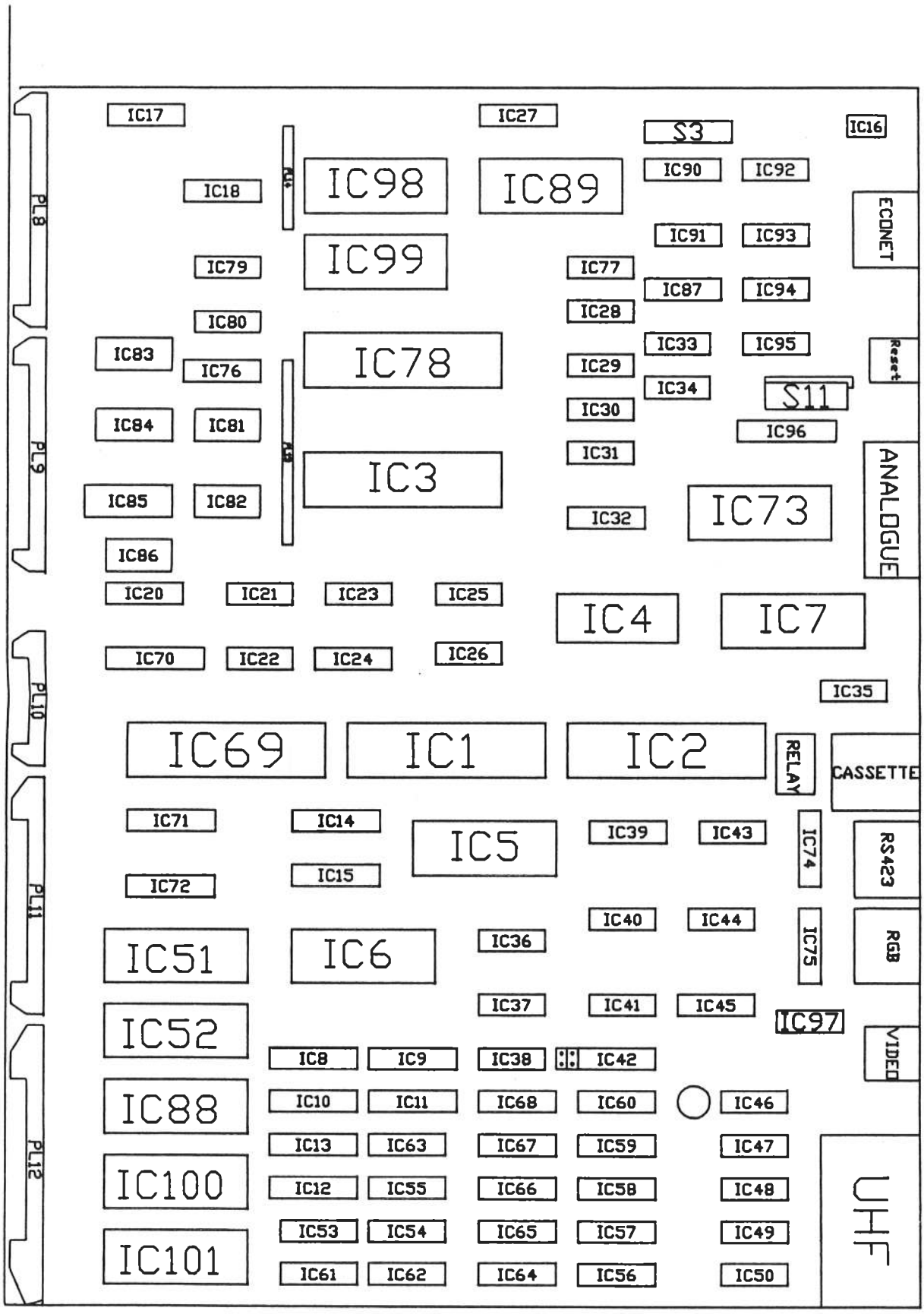
pin 9 .....

pin 10 .....

pin 11 .....



Floppy Disk Control



BBC Printed Circuit Board

Floppy Disk Control

SERIAL INTERFACE

Two forms of serial interface are provided, one is an audio cassette at either 300 or 1200 baud and the other is RS423, over a whole range of baud rates. (RS423 is electrically compatible with RS232C in most applications).

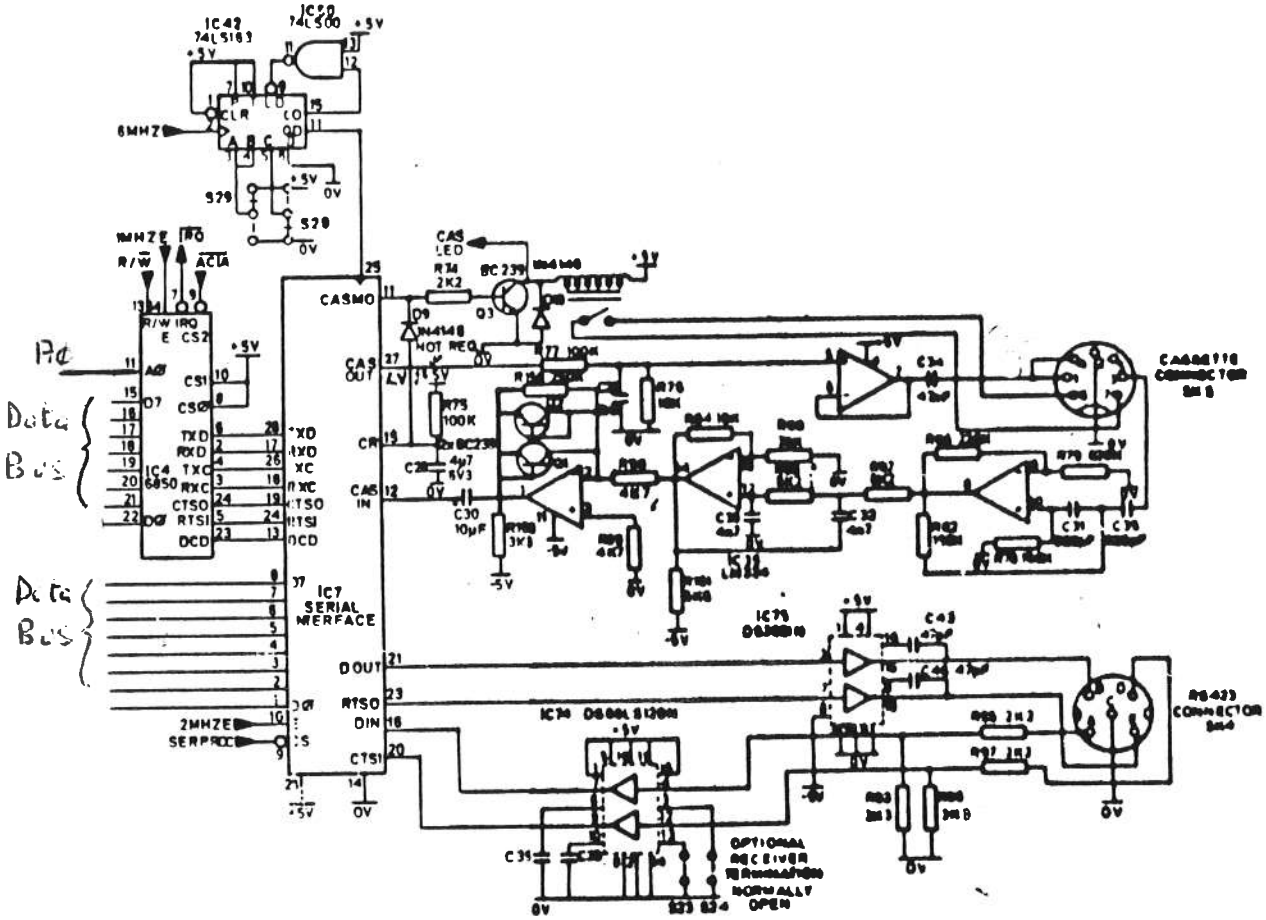
A 6850 asynchronous communications interface adaptor (IC 4) is used to buffer and serialise or deserialise the data. A second ULA specifically designed for the BBC Microcomputer is also used in the serial interface, (IC 7). Contained within this ULA is a programmable baud rate generator, a cassette data/clock separator and switching to select either RS423 or cassette operations. IC 42 divides the main board 16 MHz clock by 13 and this signal is divided further within the serial interface ULA to produce the 1200 Hz cassette signal.

Automatic motor control of an audio cassette recorder is achieved by a small relay driven by a transistor or the serial interface ULA. The signal out of the cassette is buffered and the incoming signal is suitably filtered and shaped by a three stage amplifier. This is a quad operational amplifier (IC 35). The RS423 data in and out signals and request to send and clear to send signals are interfaced by ICs 74 and 75 which translate between TTL and standard RS423/232 signal levels. Note that this is one of the few sections of circuitry on the Microcomputer which requires an additional -5v supply to be present.

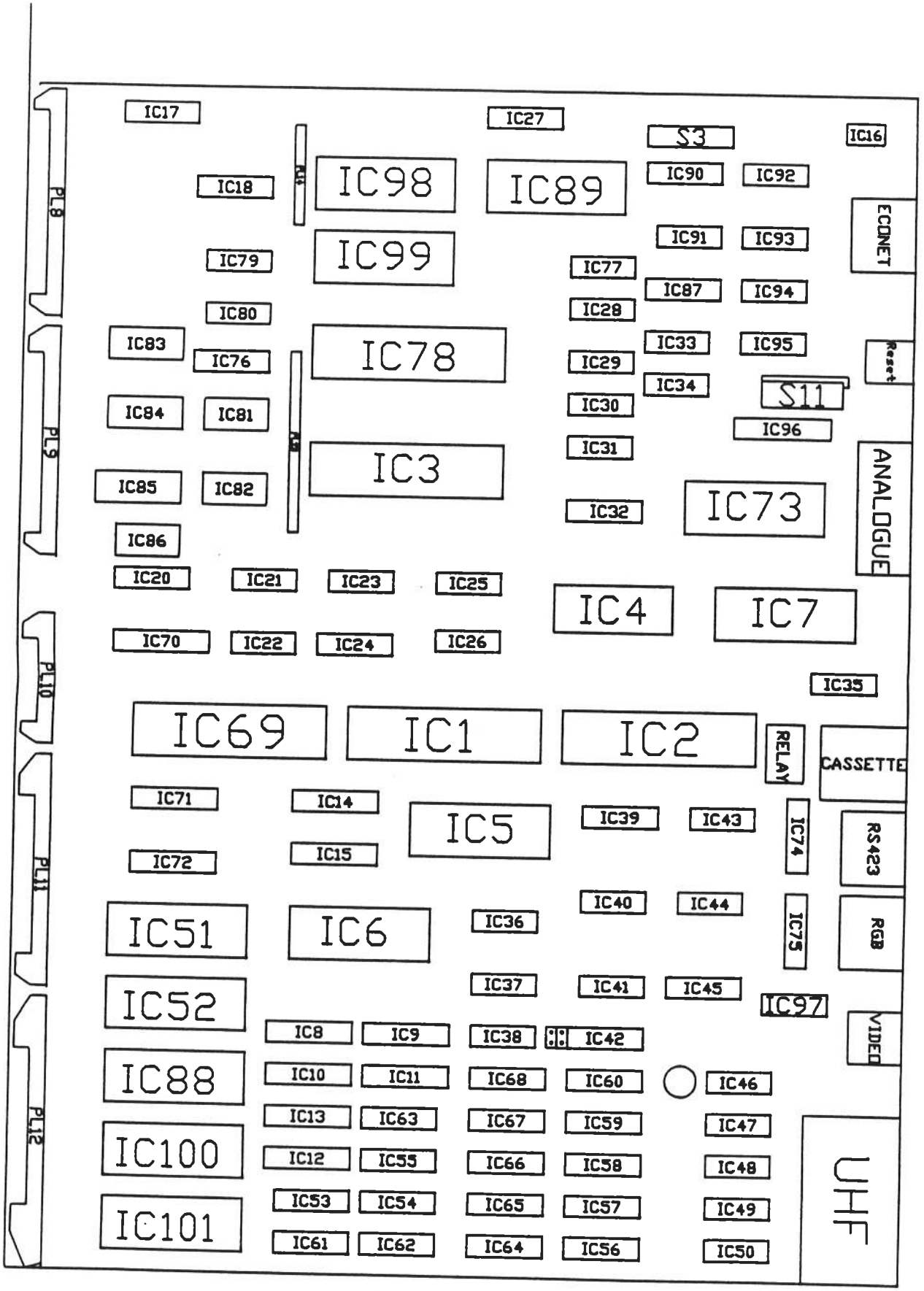
EXERCISE

Check the frequency of the signals on:

IC 7	pin 18	.....
	pin 25	.....
	pin 26	.....



Cassette and Serial Interface



BBC Printed Circuit Board

Cassette and Serial Interface

SOUND GENERATOR

The four-channel sound effects facility on the BBC Microcomputer is provided by a microprocessor-bus compatible sound generator integrated circuit type SN76489AN (IC 18). This device is accessed at 1 MHz by the system VIA (IC 3). The pitch and attenuation of each channel is therefore under the control of the microprocessor. The 4 MHz clock from the video ULA provides the clock input to the sound generator.

The audio output signal from the sound generator is mixed with the other audio signals generated by the microcomputer, thus providing a composite sound signal. This signal is then amplified and filtered using analogue circuitry based on operational amplifiers within an LM324 integrated circuit (IC 17) The resulting analogue signal is fed to PL16, which is also fed to a preset potentiometer (VR1), which acts as a volume control for the internal power amplifier of the computer. This power amplifier is a low supply voltage device, type LM386 (IC 19).

EXERCISE

Enter and RUN the following program (you may prefer to disconnect the loudspeaker first).

```
10  REPEAT
20  VDU7
30  UNTIL FALSE
```

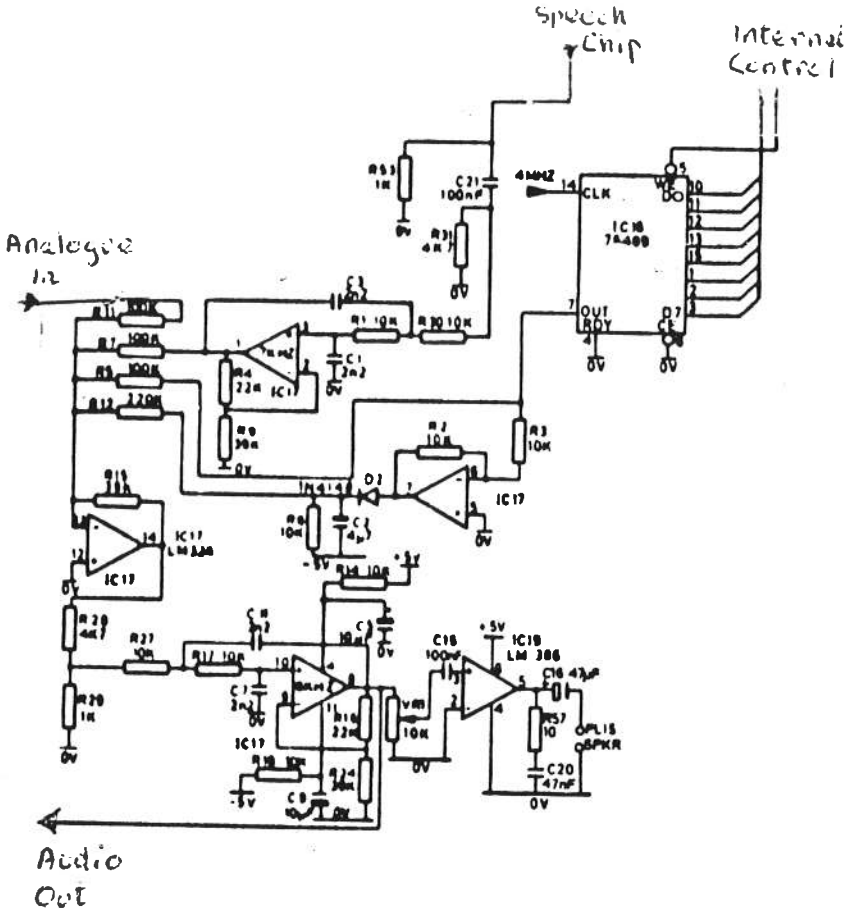
Trace the audio signal through:

IC 18 pin 7 .....

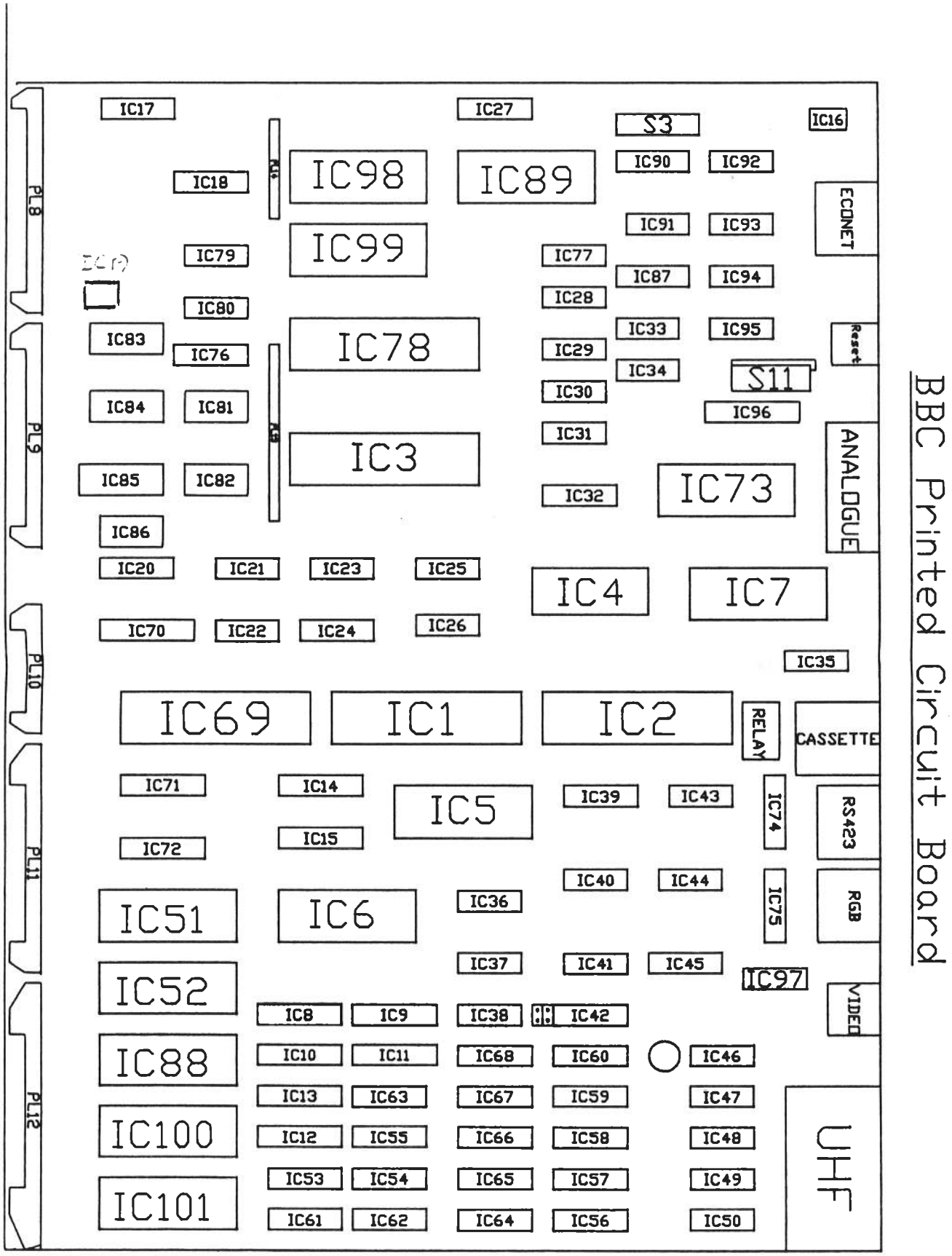
17 pin 14 .....

17 pin 8 .....

19 pin 5 .....



Sound Circuitry



BBC Printed Circuit Board

Sound Generation

S U M M A R Y

The purpose of this first section is to familiarise users with the more common sections of the micro and with setting up cyclic conditions which can be investigated using an oscilloscope and frequency meter. The tube, 1 MHz bus, Econet and voice generating circuitry is described elsewhere.