

**Servicing the BBC Micro**

**Free Run Signature Analysis**



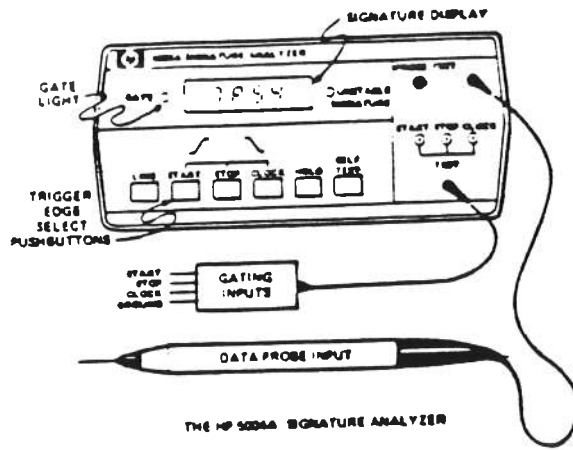
## SIGNATURE ANALYSIS

The traditional approach to fault finding in an analogue system is to produce an ANNOTATED SCHEMATIC that clearly shows the voltage levels and waveforms expected at different points within the circuit, figure (1)

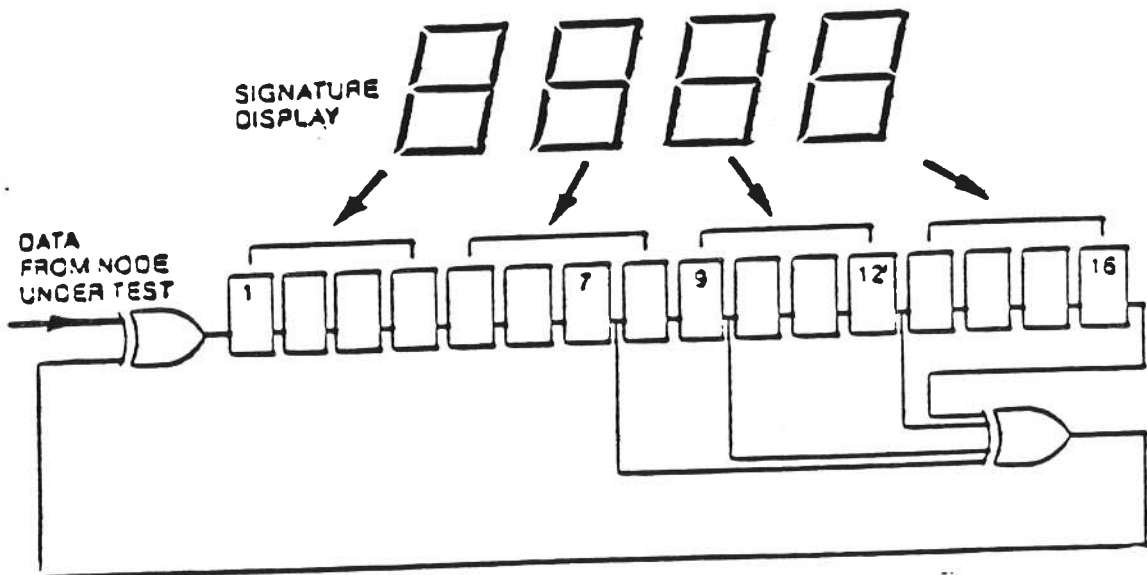
By comparing voltmeter readings and oscilloscope traces with those given on the diagram a serviceman can detect faults and make repairs without a detailed knowledge of the circuit. Adopting the same approach with digital circuits meets with several problems. Neither voltmeters nor oscilloscopes yield meaning information, voltage levels lie at either 0V or +5V, waveforms are long, complex and have a random appearance that makes all data streams look much alike.

Clearly what is required is an instrument capable of recording these complex data streams and yet able to present them to the serviceman in a compact form. The signature analyser fills this role ideally. Like the oscilloscope it monitors the logic activity at a circuit node, but instead of replaying a picture of this activity it produces a four digit code or SIGNATURE to represent the data stream, figure (2). The signature itself has no meaning and serves only as a token representing the pattern of logic ones and zeros forming the data stream. If the pattern changes, by even one bit, the signature changes.

Using signature analysis an annotated schematic for a digital circuit might look like figure (3). Instead of voltages and sample waveforms each circuit node is labelled with a signature that characterises the data stream at that point.



5 CONNECTIONS ARE MADE TO UNIT UNDER TEST.



16 BIT FEEDBACK REGISTER USED IN SIGNATURE ANALYSER

FIGURE (A) THE SIGNATURE ANALYSER

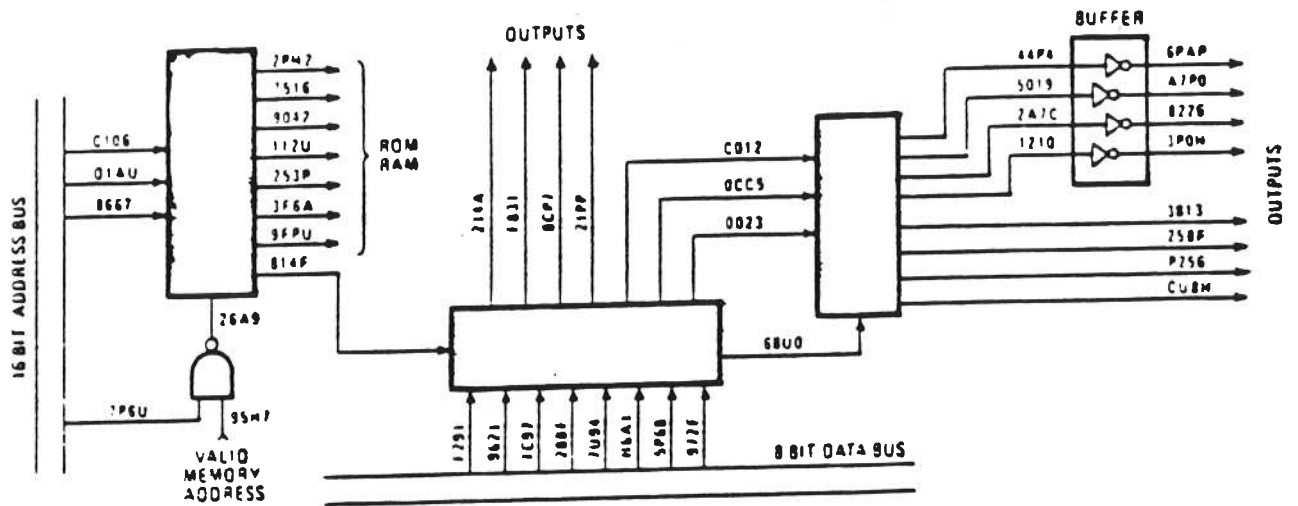


FIGURE (3) SIGNATURES DISPLAYED ON DIGITAL ANNOTATED SCHEMATIC.

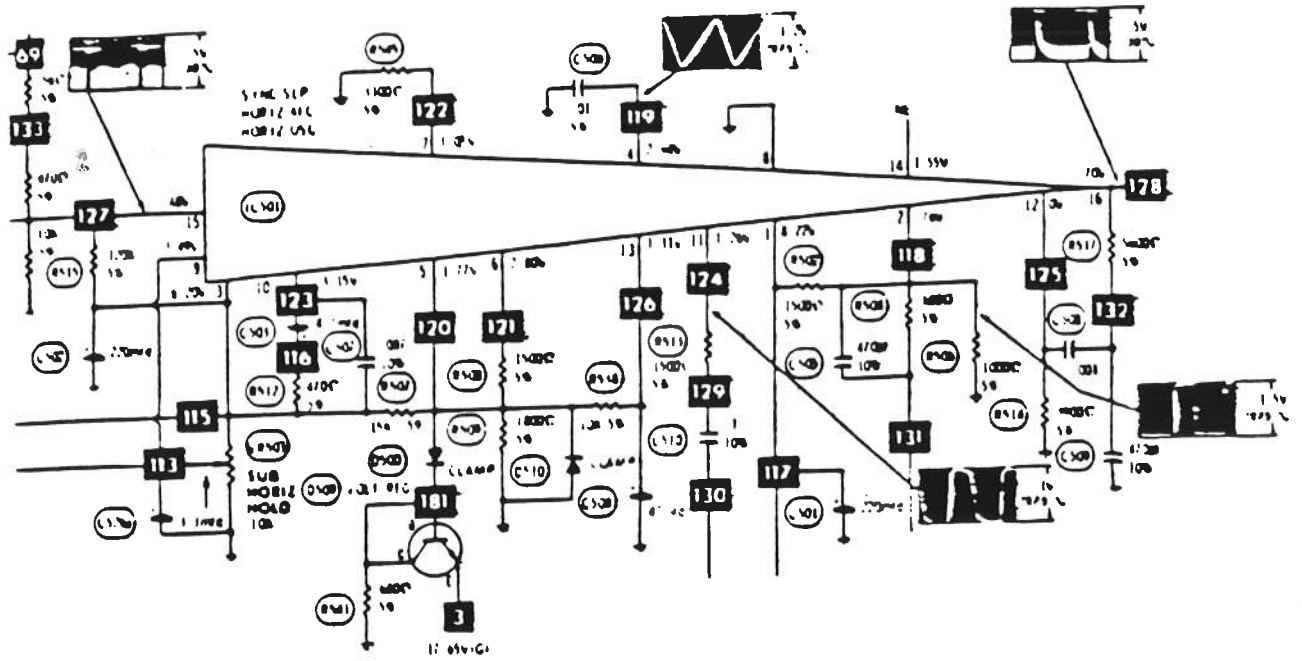


FIGURE (1) CONVENTIONAL ANNOTATED SCHEMATIC  
SHOWING VOLTAGE LEVELS AND EXPECTED  
WAVEFORMS AT DIFFERENT CIRCUIT NODES

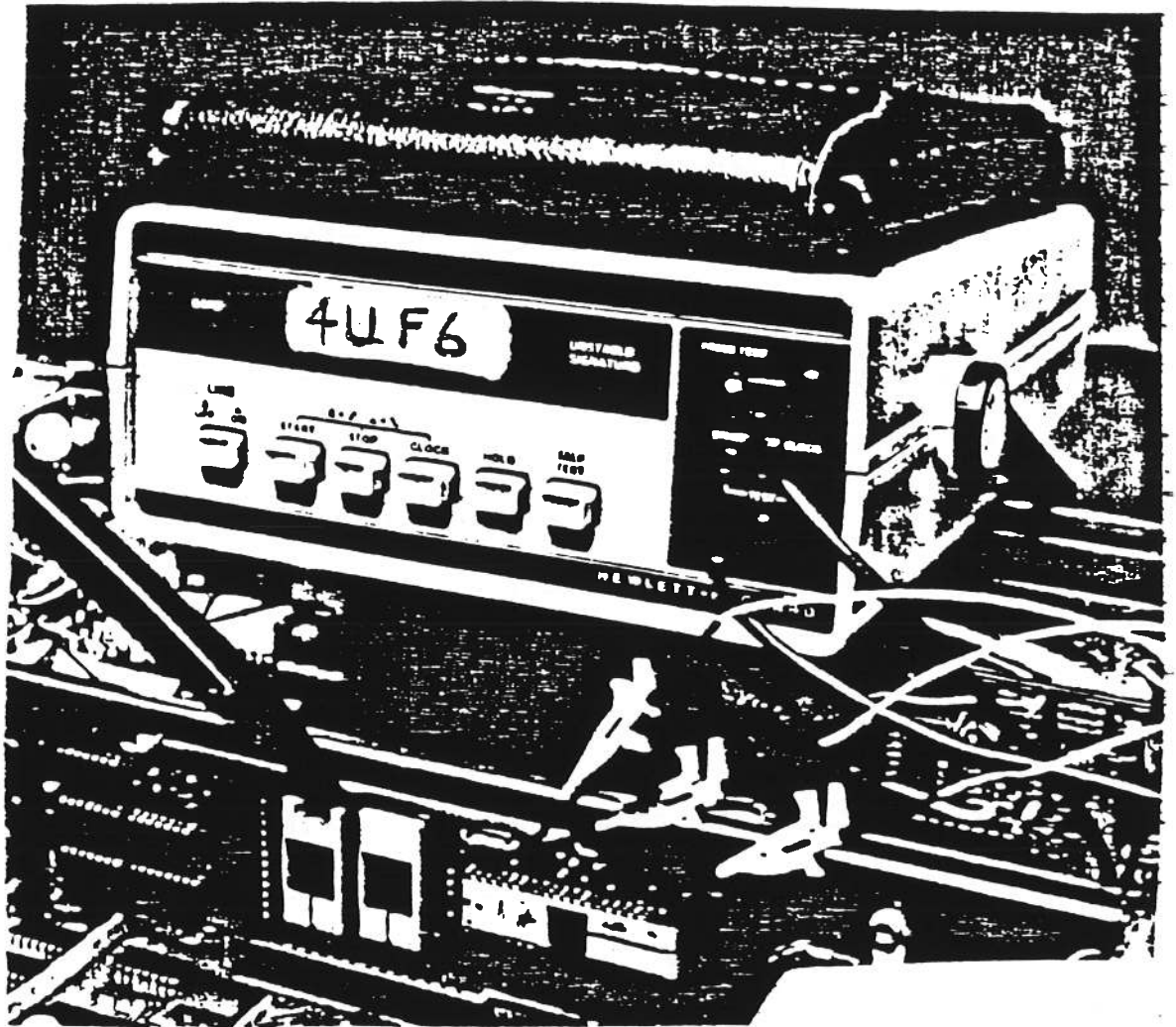


FIGURE (2) SIGNATURE ANALYSER PRODUCES A  
4 DIGIT CODE TO REPRESENT THE  
DATA STREAM.

In microprocessor based systems the activity at a circuit node and hence the signature will depend on the program being executed. An integral part of signature analysis is the STIMULUS or test program that exercises circuit components and nodes generating data streams. Only limited information can be obtained from a circuit node that remains in one state. The STIMULUS program should ensure that circuit nodes are "wiggled" between logic 0 and logic 1 creating meaningful data streams that reflect the systems performance.

### THE SIGNATURE ANALYSER

The function of the signature analyser is to monitor the logic levels at some point in a circuit and produce a code or signature that characterises the activity at that point. Figure (4) shows the layout of a typical instrument.

In operation five connections are made to the circuit under test. Data from the selected node enters the analyser directly through the data probe; the other connections START, STOP, CLOCK and EARTH are made via an external POD. Similar to the logic analyser a CLOCK signal is used to strobe data into the signature analyser. Typically clock frequencies between DC and 10 MHz are acceptable and switches on the front panel allow the operator to chose either a  $\uparrow$  or a  $\downarrow$  edge as the active transition of the clock. The START and STOP signals define the length of the data stream or the "signature window".

At the heart of the instrument lies a 16 bit shift register with feedback. On receipt of a valid START signal the register is reset to zero and data is shifted in using the selected clock edge. The feedback



paths "scramble" the data entering the register and ensure that all the bits forming the data stream, not just the last sixteen, contribute to the final signature. On receipt of a STOP signal the 16 bits remaining in the register are displayed in a hexadecimal format to give the signature of the observed data stream.

A non-standard hexadecimal character set    0 1 2 3 4 5 6 7 8 9  
A C P H P U    is used to display the signature code. This set has two advantages over the standard code:-

1. EACH character can easily be reproduced on a 7 segment LED display with none of the confusion between 6 and small b or 8 and capital B found in the standard set.
2. The operator is not tempted to confuse the 4 digit hex with system addresses or to work backwards from the signature in search of further information.

Two LED indicators labelled GATE and UNSTABLE SIGNATURE give information on the signals used by the analyser. The GATE light turns on when the window opens and off when it closes. If the window is continuously opening and closing the GATE light flashes at about 10Hz. The UNSTABLE SIGNATURE flashes if the signatures obtained in successive windows differ.

#### A CLOSER LOOK AT THE SIGNATURE WINDOW

The signature window is controlled by the three inputs START, STOP and CLOCK. In operation these signals can be provided by the circuit under test. To allow flexibility the active or trigger edges for each signal can be selected by the controls on the front panel of the analyser.

Normally the CLOCK edge is chosen to define a time when data is stable on the selected node. The logic state of the node is sampled only at the CLOCK edge and ignored at all other times. The CLOCK is also used together with the START and STOP signals to define the signature window or gate. Figure (5) shows that a CLOCK edge is required both before and after the START and STOP edges for the instrument to detect the change in state of these inputs.

Notice the window opens not at the START edge but at the CLOCK edge following the START edge. In the same manner the window closes at the CLOCK edge following the STOP edge. The first piece of data to enter the shift register occurs at the first CLOCK edge following the START edge. The final data bit is clocked into the analyser by the clock edge prior to the stop edge.

Gating signals must be chosen with care to ensure proper opening and closing of the signature window. The diagrams given in figure (6) illustrate the problems that can arise from a bad choice.

The solartron locator provides two triggering modes to ease the problem of forming the signature window. Mode 1 is the normal mode that requires a CLOCK edge before and after the change in state of the START and STOP signal. However, if suitable long-duration START and STOP signals are not available MODE 2 will allow triggering with signals less than one half cycle of the clock. Although this situation is less satisfactory (random pulses could cause spurious gating leading to unstable signatures) it may be the only method by which signatures can be obtained from the system under test.

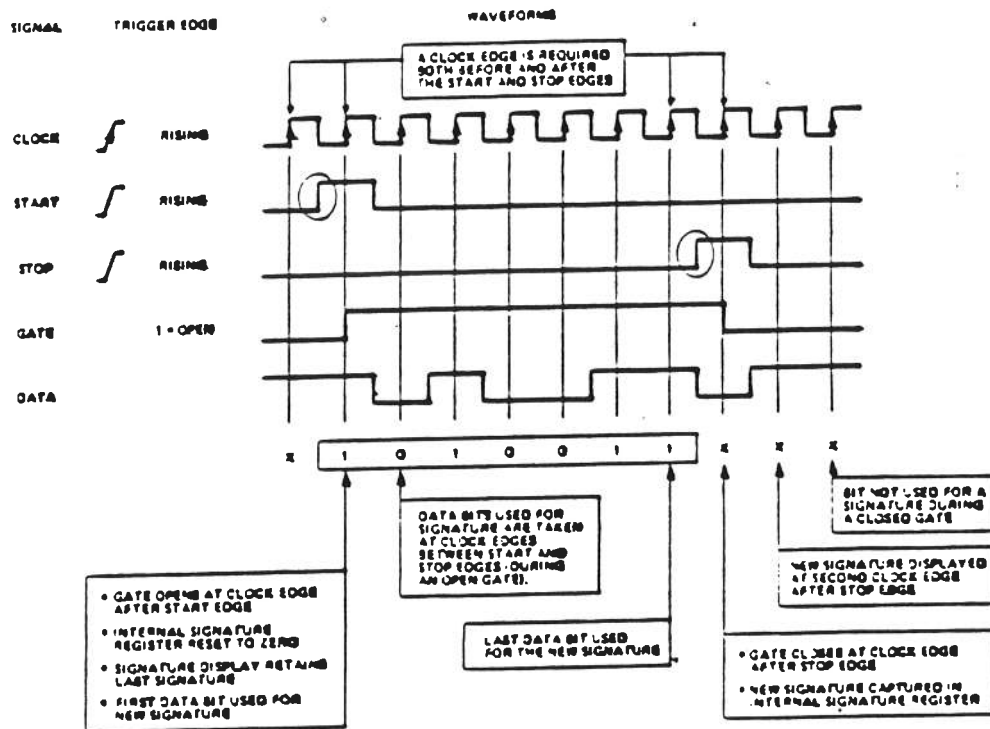
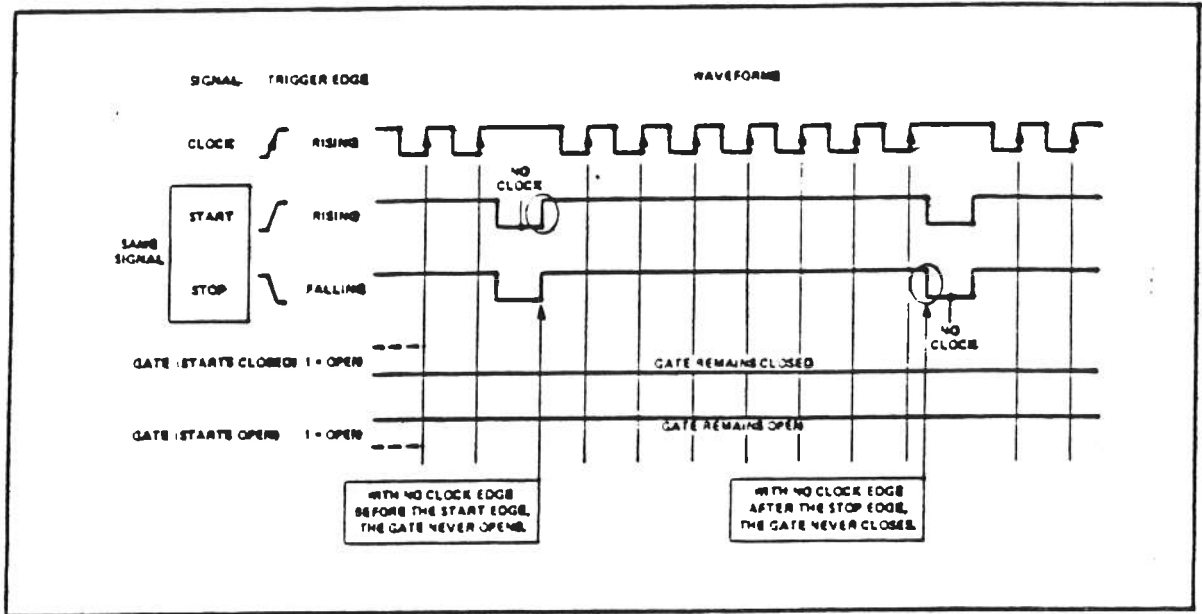


FIGURE (5) FORMING THE SIGNATURE WINDOW

(NOTE. HOW A CLOCK EDGE IS REQUIRED BOTH BEFORE AND AFTER THE START AND STOP EDGES.)

1: No CLOCK before or after the START or STOP edge.

In Figure 4.1, START and STOP are connected to the same signal and trigger on opposite edges. There is no CLOCK edge to detect the logic LOW level of START/STOP, so the rising edge for START does not open the GATE. Similarly the falling edge for STOP won't close the GATE if it starts open.



2: The START or STOP pulse is too short for the CLOCK frequency.

In the example of Figure 4.7, the STOP pulse is too short for the slower CLOCK frequency. The GATE remains open because the STOP edge is not detected. This can occur when START and STOP are connected to address decodes, and pulsed at the beginning and end of the stimulus program. If a CLOCK is chosen that is slower than the pulses, such as a UART's transmitter clock input, then the pulses will remain undetected. To get the GATE to open and close, choose a higher frequency CLOCK, or create new START and STOP edges by controlling a bit in a latch as shown in the previous example, or using the address decode pulses to set and reset a flip-flop or latch directly.

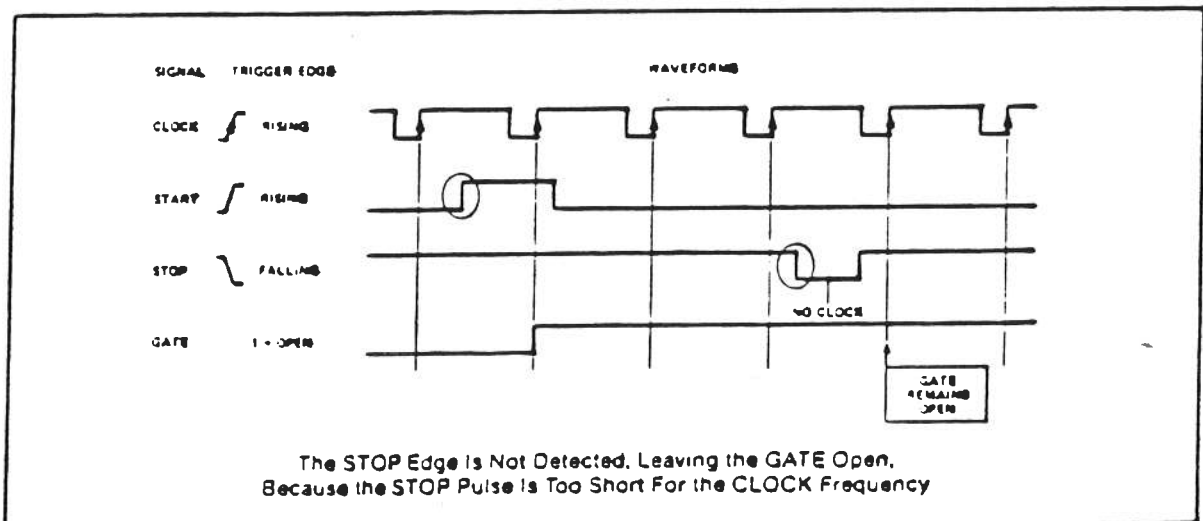
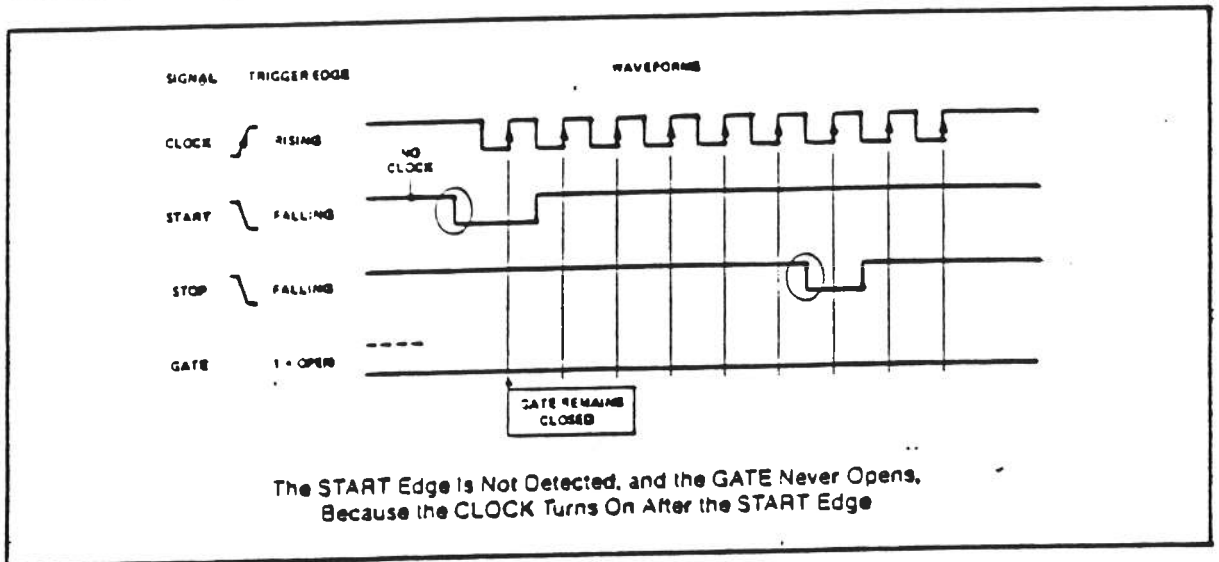


FIGURE 6) PROBLEMS THAT CAN ARISE WITH A BAD CHOICE OF SIGNATURE WINDOW.

3: The CLOCK turns on after the START edge.

In figure 4.8, the START edge is not detected because it occurs before the first CLOCK edge. This can happen in board test systems, where START is the signal from the board tester that turns on the CLOCK to the board under test. Here, selecting the other edge for START will allow the GATE to open. Choosing a CLOCK that is running before the START edge will also ensure its detection.



4: The CLOCK turns off before the STOP edge.

In Figure 4.9, the STOP edge is not detected because it occurs after the last CLOCK edge. In this example, STOP is the terminal count output of a counter. When the terminal count occurs, the counter's clock is turned off. Connecting CLOCK to the counter's clock will cause the STOP edge to remain undetected. To ensure detection, the CLOCK should be moved to a clock that runs after the STOP edge.

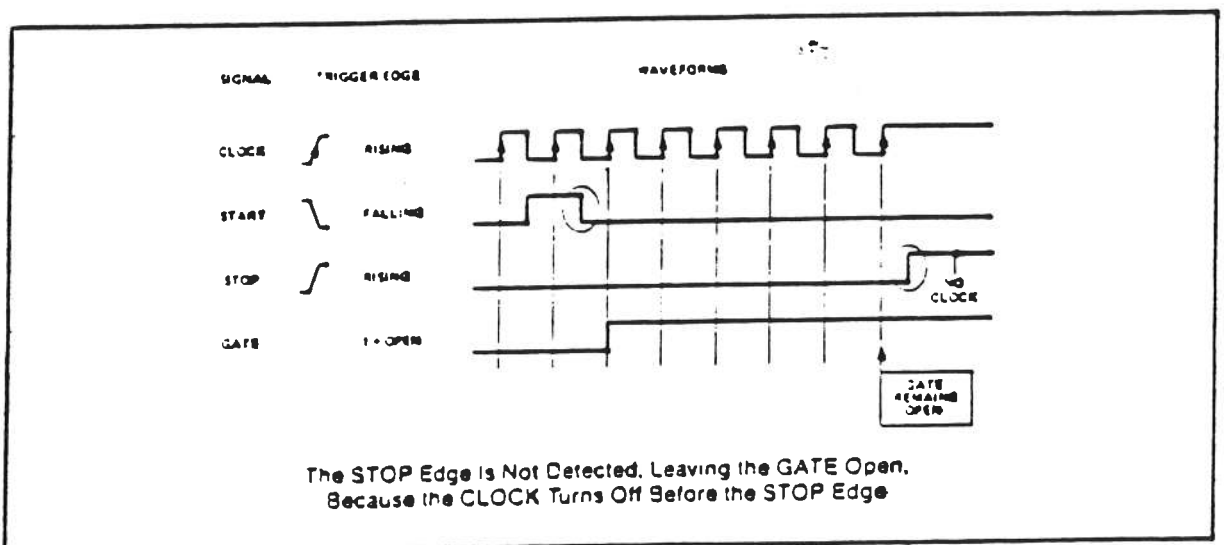


FIGURE (6) CONTINUED

## VCC, VSS SIGNATURES

A look in some detail at how the analyser deals with two simple data streams should help illustrate the function of the feedback shift register. Consider first a data stream constantly at ground potential. At each CLOCK edge a logic zero enters the analyser. As the feedback mechanism is also delivery logic zeros to the exclusive OR gate at the input of the shift register the register remains filled with zeros. Therefore the signature of a node at ground potential is always 0000. If, however, the probe monitors a point constantly at logic one the contents of the register will change as the feedback algorithm alters the bit stream entering the register.

The final signature depends only on the number of clock pulses within the signature window. For this reason the Vcc signature is often used as a preliminary check on the gate to ensure the correct number of clock edges are occurring between the START and STOP signals before proceeding to measurements on more complicated data streams.

## FREE-RUNNING AS A SOURCE OF STIMULUS

Free-running a microprocessor provides a simple method of exercising a microcomputer circuit. In this case the 6502 microprocessor in a BBC Micro is induced to free-run by "hardwiring" the code for No Operation (EA) on its data bus pins. Figure (7) shows how this is achieved. The 6502 CPU is removed from its socket and plugged into an MEDC pod, with code EA switched to the data lines. The pod is in turn connected to the BBC PCB via the vacant CPU socket. This has the following effects:

1. Disconnects the microprocessor from the system data bus preventing it from executing the system program.
2. Provides the NOP code at every address forcing the processor to cycle through its entire address range.
3. The address and control pins remain connected to exercise the address bus and any address decode circuiting on the board.

After reset the processor reads the NOP code upon which it increments the program counter and the address bus to attempt a read operation at the next location. As NOP appears at each address the microprocessor cycles through its entire address range, exercising the address decode circuitry and drawing data from the ROM and RAM chips onto the data bus generating data streams suitable for testing by signature analysis.

#### **AN EXAMPLE -**

This example illustrates the use of a free-run test module with the 6502 based BBC circuit. The example gives details of implementing signature analysis, describing the signals used by the analyser and outlining the preparation of the documentation that forms the basis of future testing.

#### **ADDRESS BUS - DECODE LOGIC SIGNATURES**

Address bus line A15 provides the necessary START and STOP signals for the signature window. Figure (2) shows its behaviour as the processor increments through its address range

1. On reading address 8000H, A15 toggles high and remains high until FFFFH after which it falls low at the start of a new scan.

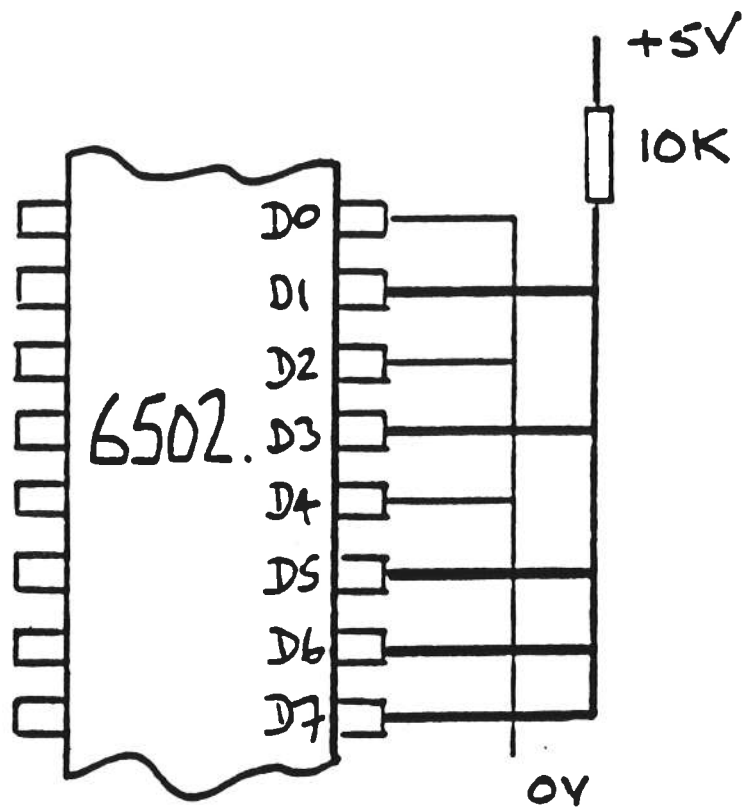


Fig 7 Data connections for 6502 free run.



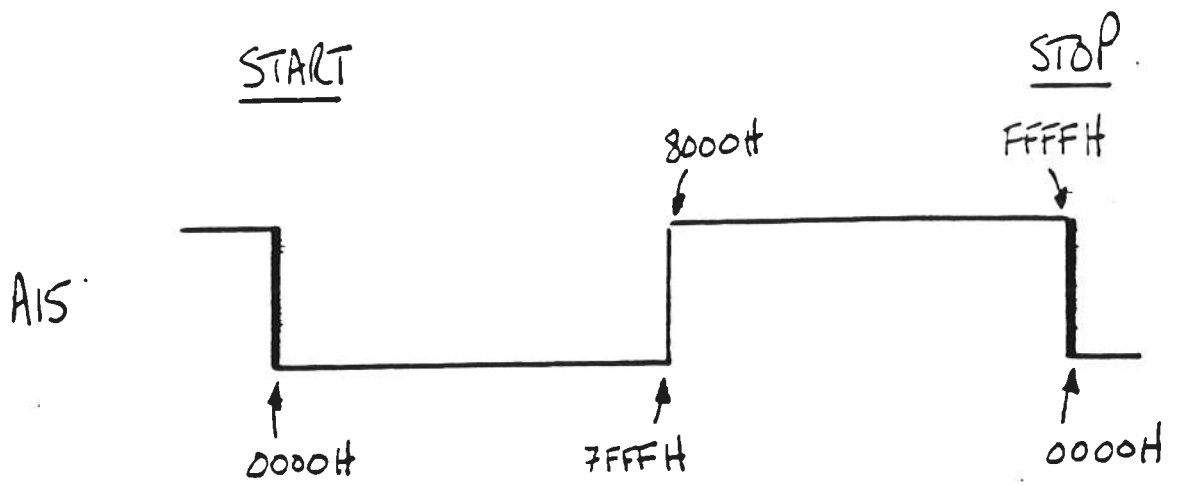


FIGURE (8) ADDRESS LINE A15 PROVIDES THE SIGNATURE WINDOW FOR THE FREE-RUN ADDRESS BUS SIGNATURES.

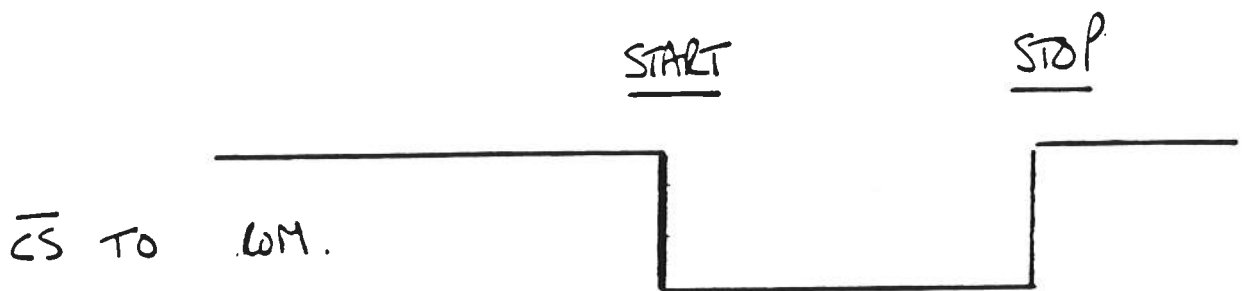


FIGURE (9) ROM CS SIGNAL FORMS THE SIGNATURE WINDOW FOR THE FREE-RUN ROM SIGNATURES.

Choosing falling edges for the START and STOP signals defines a signature window in which the processor places all possible addresses on the bus.

With the 6502 the rising edge of the  $\phi_2$  strobe defines a time at which the address is established and stable. Using it as the CLOCK input for the analyser ensures that only valid addresses are seen by the analyser.

The address bus and decode logic signatures obtained are shown in figure (9). This style of signature documentation offers an alternative to the annotated schematic. It includes details of the stimulus exercising the circuit, the signals used for CLOCK, START and STOP and the configuration of the analyser. The Vcc signature is given at the start of the table, the ground signature is always 0000. Next to each circuit node is listed the components visited by the line and their characteristic signature.

#### ROM SIGNATURES

In the free-run mode, the microprocessor attempts to read every possible address drawing information from the system memory onto the data bus and generating data streams that characterise memory contents. The break in the data bus formed by the free-run module prevents any of this information reaching the processor and also separates the NOP code at the processor from the system bus. However, before taking signatures on the data bus two changes are required. Firstly, to observe data as

opposed to address the CLOCK used by the analyser has to be moved to a different place in the timing cycle, namely to the falling edge of the  $\Phi_2$  strobe. Secondly, leaving the signature window to encompass the processor reading the entire 64k would yield signatures formed by ROM and RAM. As there is no simple method of ensuring the system always powered up with the same RAM contents these signatures would be unrepeatable and therefore useless. However, meaningful signatures can be obtained if the signature window is redefined to enclose only data streams from the system ROM. Figure (10) shows how this is achieved by connecting the START and STOP inputs to the chip select signal to a ROM Chip Select Signal.

*for a typical ROM*

The eight data bus signatures are shown in figure 11. Again each IC visited by the data bus is shown beside each node. A further point worth attention is that changing the signature window from the previous test has resulted in a new value for the Vcc signature.

#### SUMMARY

Free-running the microprocessor provides a relatively simple method of stimulating a large part of a microcomputer system thereby enabling testing by signature analysis. Signatures taken on the address bus and the decode logic serve as a means of verifying their operation. Data bus signatures not only provide a check on the operation and contents of ROM but also on possible defects on the bus e.g. lines stuck or shorted, solder bridges or devices with outputs permanently enabled etc.

MEDC SIGNATURE REPORT FORM

TITLE: BBC Micro Free Run

FUNCTION : START : STOP : CLOCK : MODE : VCC : START : STOP : CLOCK  
 Address & : 7 : 7 : 5 : 1 : SIGN : ID : ID : ID  
 Chip Select : : : : : C003 : AB15 : AB15 : 02







CLOCK QUALIFIER : : : : : : :

NODE	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	SIGNATURE
AB0	IC1 Pin9	IC73 Pin6	IC4 Pin11	IC6 Pin2	IC25 Pin10	0000
	IC52 Pin10	IC51 Pin10	IC28 Pin10	IC100 Pin10	IC101 Pin10	
	IC3 Pin33	IC72 Pin21	IC69 Pin38			
AB1	IC1 Pin10	---	---	---	---	FFFF
AB15	IC1 Pin25	--	--			0001
CS(1)	IC51 Pin20					755F
CS(2)						

Fig. 10

MEDC SIGNATURE REPORT FORM

TITLE: BBC Micro Free Run

FUNCTION : START : STOP : CLOCK : MODE : VCC : START : STOP : CLOCK  
 BASIC ROM :  :  :  : 1 : 755U :  $\overline{CS}$  :  $\overline{CS}$  :  $\Phi_2$   
 Data :  :  :  : 1 : 755U :  $\overline{CS}$  :  $\overline{CS}$  :  $\Phi_2$

CLOCK QUALIFIER : : : : : :

NODE	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	CIRCUIT ID	SIGNATURE
DB $\phi$	IC52 Pin 11	IC69 Pin 33	IC78 Pin 12	IC3 Pin 33		320U
DB7	IC52 Pin 1	IC69 Pin 26	IC78 Pin 19	IC3 Pin 26		71PU

Fig 11









**Servicing the BBC Micro**

**Free Run Signature Analysis**

**Practical**

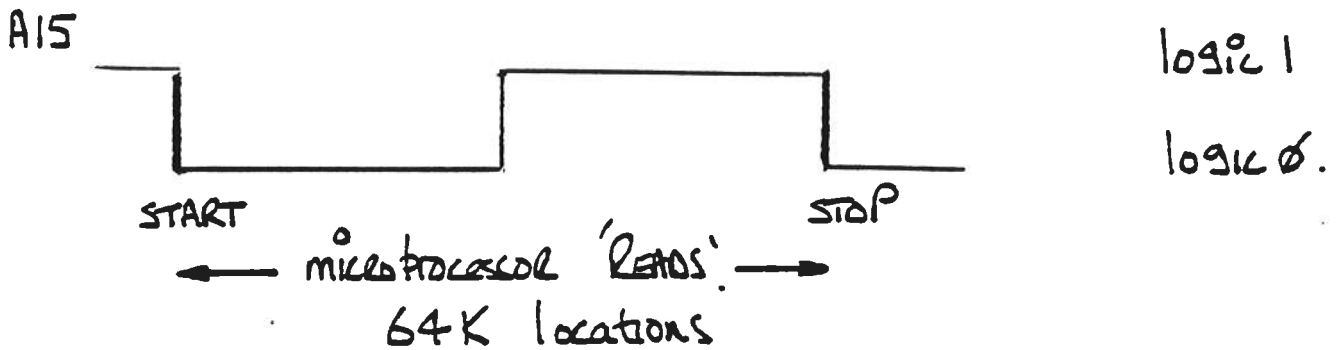


EXPERIMENT 1 - Free-running the Microprocessor - address bus and decode circuitry signatures.

APPARATUS - BBC micro, 7201 Solartron Locator.

### INTRODUCTION

This experiment uses the free-run module to induce the microprocessor to index its address lines through the entire 64K of the system's memory map. The technique provides a simple method of stimulating the address bus and the decode circuitry, generating signatures. Address line A15 provides the START and STOP signals. The rising edge of the  $\phi_2$  clock is used to clock data into the signature analyser.



### PROCEDURE

(1) With the BBC switched off, carefully remove the CPU and insert the 'free-run' module.

(2) Connect the Right Data Pod terminals as follows:

START (green) A15

STOP (red) A15

COMMON (black) Vss

CLOCK (yellow)  $\phi_2$

(3) Switch on the locator and set up as follows:

(a) Select SIGNATURE

(b) Start trigger polarity

(c) Stop trigger polarity

(d) Clock polarity

(e) Mode



- (4) Switch on the BBC . The gate indicator should flash to indicate that a signature gathering window is occurring.
- (5) Vss signature. Touch the logic probe to ground and observe that the signature is 0000. This is the characteristic logic zero signature for ALL test set ups.
- (6) Vcc signature. Touch the logic probe to Vcc and take the Vcc signature. This signature is characteristic of THIS ARRANGEMENT ONLY. It serves as a check on the signature window. Record this signature in the following chart.
- (7) Take signatures on address bus pins A0 - A15 and verify these signatures at each chip visited by the address bus. Again note your results in the following chart.
- (8) Take signatures on the chip select pins of the memory devices present in your micro.
- (9) Compare your results with those obtained by your neighbour.

The documentation you have produced will serve as a reference of good signatures from a working system.

Note - The BBC Micro may give a continuous sound output in free run. If this occurs disconnect the speaker



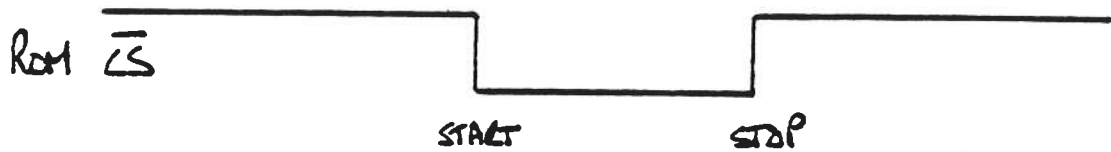


EXPERIMENT 2 - Free-running the microprocessor, using the signature analyser to check ROM.

APPARATUS - BBC Micro, 7201 Solartron locator.

### INTRODUCTION

Again the free-run module is used to induce the microprocessor to read all possible addresses. However, in this test the analyser is gated to look only at the data stream on the data bus while a ROM is being addressed. This is achieved using the falling edge of the chip select (cs) signal to the ROM under test as a START signal and the rising edge at the end of selection as the STOP signal.



Note - This technique does not work for the operating system ROM because of the memory mapped I/O

### PROCEDURE

1. With the BBC switched off, connect up the right Data Pod as follows:

START (green)	$\bar{CS}$ ROM
STOP (red)	$\bar{CS}$ ROM
COMMON (black)	V <sub>SS</sub>
CLOCK (yellow)	$\phi_2$

2. Set up the locator as follows:

(a) Select Signature

(b) Start Trigger Polarity



(c) Stop Trigger Polarity



(d) Clock Polarity



(e) Mode

1

3. Switch on the BBC and take the Vcc signature.
4. Take Signatures on each Data Bus Pin.









